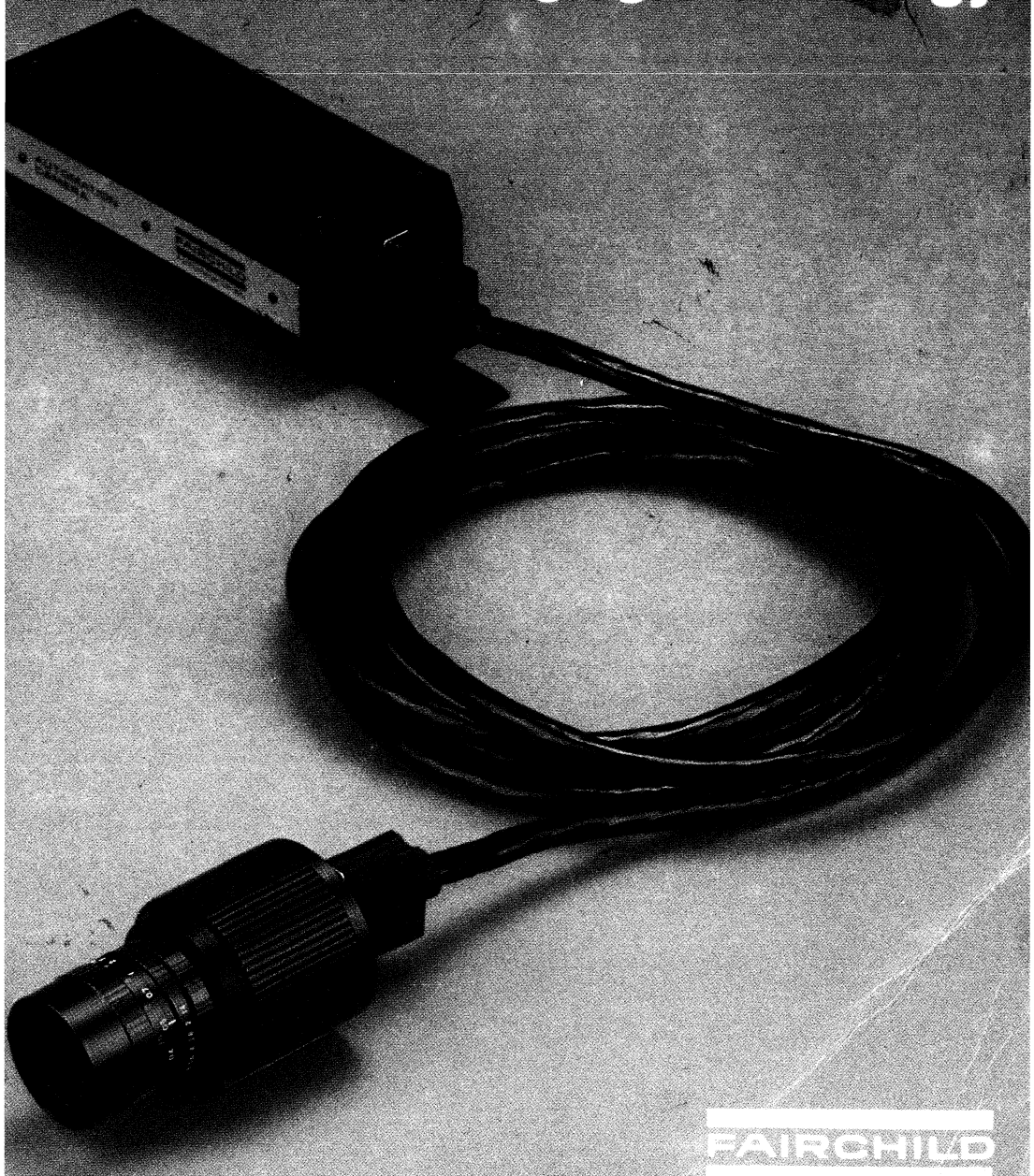
CCD

The Solid State Imaging Technology



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During the '70s, Fairchild led the development of CCD Technology. Since the beginning, the buried-channel concept has been utilized in all CCD products. The product line therefore exhibits all the advantages of buried-channel technology including low noise, high speed and high density.

Transferring this process from an R & D operation to a volume production environment required extensive efforts in research, design, development and production engineering. Our efforts paid off. Fairchild leads the way in CCD technology.

Fairchild CCD Imaging offers a broad product line. Specifically, we offer line scan sensors with 256 to 3,456 elements of resolution. We carry a full line of both line scan and area cameras. In addition we have a new line of vision interface processors. We also offer signal processing devices including video delay lines.

The '80s is the CCD Decade. And Fairchild is the CCD Leader.

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INTRODUCTION

Line Scan Image Sensors

Basically, a line scan image sensor is composed of a row of image sensing elements (photosites), two analog transport registers, and an output amplifier. Light energy falls on the photosites and generates charge packets proportional to the light intensity. These charge packets are then transferred in parallel to two analog transport registers, which are clocked by 2-phase clocks. The packets are next delivered to an on-chip output amplifier where they are converted to proportional voltage levels. A series of pulses, amplitude modulated with the optical information, appear at the output.

Key advantages of Fairchild CCD line scan sensors, due to Fairchild's Isoplanar buried-channel structure, include high data rates, high charge transfer efficiencies, low noise, and relatively small die sizes.

Line scan sensors find applications ranging from optical character recognition (OCR) using the 256 × 1 device to facsimile sensing using the 1728 × 1 or 3456 × 1 device. The precise location of the photosites on the sensor allows the device to be used in high precision non-contact measurement applications such as dimensional measurements of objects, shape recognition and sorting, and defect detection.

The following tables summarize the features of Fairchild's Line Scan Imaging Products.

Line Scan Sensor

Order Code	Number of Elements	Element Size	Maximum Data Rate	Range (Typical)	Responsivity (Typical)
CD111ADC	256×1	13×17 microns	10 MHz	2500:1	1.3 V per μj/cm²
CD111BDC	256×1	13×17 microns	10 MHz	2500:1	1.1 V per μj/cm²
CCD112DC	256×1	13×13 microns	5 MHz	5000:1	3.0 V per μj/cm²
CCD133DC	1024×1	13×13 microns	20 MHz	5000:1	3.0 V per μj/cm²
CCD134DC	1024×1	13×13 microns	20 MHz	5000:1	3.0 V per μj/cm²
CCD122DC	1728×1	13×13 microns	2 MHz	2500:1	3.5 V per μj/cm²
CCD123DC	1728×1	10×13 microns	2 MHz	2500:1	3.5 V per μj/cm²
CCD143DC	2048×1	13×13 microns	20 MHz	5000:1	3.0 V per μj/cm²
CCD145DC	2048×1	13×13 microns	8 MHz	2500:1	4.0 V per μj/cm²
CCD151DC	3456×1	7×7 microns	5 MHz	2500:1	4.0 V per μj/cm²

Line Scan Design Aids (do not include sensors)

Order Code	Sensor Supported	Comments
I-SCAN*	CD111ADC	Fairchild offers a series of printed circuit boards for use as construction aids for experimental systems using CCD line scan image sensors. These design and development boards are fully assembled and tested, and require only power supplies and an oscilloscope to display the video information corresponding to the image positioned in front of the sensor.
CCD133DB	CCD133DC	
CCD122DB	CCD122DC	
CCD143DB	CCD143DC	
CCD151DB	CCD151DC	

* I-SCAN includes CD111ADC.

Camera Subsystems

Fairchild CCD camera subsystems are fully assembled and calibrated electro-optical instruments useful in a wide variety of scientific and industrial applications.

Each subsystem is comprised of a camera, a line-powered control unit, and interconnecting cables. The camera, which may be ordered separately, may be equipped with a lens suitable for the application.

Line Scan Camera resolutions of 256, 512, 1024 and 2048 elements per line are available. Line scan subsystems are particularly useful for acquisition of optical data for objects in motion, i.e., facsimile scanning of documents transported past the camera's field of view or measurement of objects carried past a camera inspection station on a conveyor belt. Typical subsystem applications include microfiche and microfilm scanning, document scanning for mark sensing, facsimile transduction and OCR data acquisition; precision non-contact measurement and inspection, flaw detection, shape analysis, dimensional measurement, color sorting; and for a wide variety of laboratory uses.

Area Cameras are ideally suited for industrial environments. The CCD3000 Video Communications Camera provides standard television output signals for display of high-resolution images on low-cost monitors or for digital analysis using NTSC image processing equipment. The CCD3000 is also available with a fiber optic faceplate for interfacing to customer fiber optic image inputs as well as with an image intensifier for low light level applications. The CCD4001 Robotics Camera provides image data output in a non-interlaced 256 by 256 element square pixel pitch format which can be utilized by a CPU for automatic inspection, recognition and robot guidance. All Fairchild area cameras can be used as a relatively small single-component camera, or be separated into a camera control unit plus a cable-connected sense head which is robust enough to be mounted onto a robot arm.

Commercial Line Scan Camera System

Includes Camera Control Unit and Interconnect Cables.
Camera only may be ordered as CAM1100C, CAM1200C, CAM1300C, CAM1400C or CAM1500C.

Order Code	Number of Elements	Line Scan Rate	Exposure Time	Data Rate
CCD1100C	256×1	60 Hz - 35 KHz	30 μs - 16 ms	100 KHz - 10 MHz
CCD1200C	512×1	60 Hz - 20 KHz	51 μs - 16 ms	100 KHz - 10 MHz
CCD1300C	1024×1	60 Hz - 10 KHz	102 μs - 16 ms	100 KHz - 10 MHz
CCD1400C*	1728×1	60 Hz - 6 KHz	175 μs - 16 ms	100 KHz - 10 MHz
CCD1500C	2048×1	60 Hz - 5 KHz	204 μs - 16 ms	100 KHz - 10 MHz

*The CCD1400C and CAM1400C are being discontinued. Stock is currently available in small quantities.

Industrial Line Scan Camera System (camera only)

Order Code	Number of Elements	Max. Line Scan Rate	Min. Exposure Time	Data Rate
CCD1200R	512×1	38 K lines/sec	26 μs	100 KHz - 20 MHz
CCD1300R	1024×1	19 K lines/sec	52 μs	100 KHz - 20 MHz
CCD1500R	2048×1	9.7 K lines/sec	103 μs	100 KHz - 20 MHz

Area Camera Systems

Includes Camera, Power Supply and Remote Sense Head Cable.
Camera only may be ordered as CAM3000, CAM3100, CAM3000F, CAM3100F or CAM4001.

Order Code	Scanning format	Comment
CCD3000	Full 488×380 NTSC Resolution	
CCD3100	Full 488×380 NTSC Resolution	222A Sensor
CCD3000F	Full 488×380 NTSC Resolution	Fiber Optic Faceplate
CCD3100F	Full 488×380 NTSC Resolution	222A and Fiber Optic Faceplate
CCD4001	256×256 Non-Interlaced	

Camera Accessories

Order Code	For use with	Description
LENS13C	All (except CCD1500)	13 mm Lens, Standard C Mount
LENS25C	All (except CCD1500)	25 mm Lens, Standard C Mount
LENS50C	All (except CCD1500)	50 mm Lens, Standard C Mount
LENS28B	CCD1500C, CCD1500R	28 mm Lens, Bayonet Mount
LENS50B	CCD1500C, CCD1500R	50 mm Lens, Bayonet Mount
CNTRLINE	Comm. Line Scan Camera	Control Unit with Interconnect Cables
CABLE	Comm. Line Scan Camera	Interconnect Cables only
CABLAUTO	CCD3000, CCD3000F	Remote Sense Head Cable for CCD3000
CABL4001	CCD4001	Remote Sense Head Cable for CCD4001
PWRSPLY	CCD3000	Power Supply
PIX1100	CCD1100C	Pixel Locator
PIX1200	CCD1200C	Pixel Locator
PIX1300	CCD1300C	Pixel Locator
PIX1400	CCD1400C	Pixel Locator
PIX1500	CCD1500C	Pixel Locator
MONITOR	CCD3000, CCD4001	NTSC Monitor, Black and White

Vision Interface Processor

In many applications there is a need for decision-making based on the data from CCD cameras rather than just for a display of imagery. To yield a decision, the camera data must first be converted from analog to digital and subsequently interpreted. Fairchild's multibus* formatted VIP100 Vision Interface Processor accepts analog video from any Fairchild CCD camera. It converts the analog video to binary and then processes the converted data, which enables it to perform a host of industrial inspection and robotic vision system functions. Processing is accomplished using the on-board 16-bit 20MHz Fairchild F9445 microprocessor. Applications include Non-Contact Measurement, Defect, Surface Flaw and Edge Flaw Detection, Automated Parts sorting, OCR, Shape and Pattern Recognition, Object Recognition and Robot Guidance.

This versatile board is capable of being used as a stand alone processor or as part of a larger system using the link to the multibus, either of two RS-232 ports or separate user configurable 16-bit data input and output ports.

Computer Interface Systems

Order Code	For use with	Description
VIP100-20	All Fairchild cameras	Vision Interface Card with 20 MHz F9445

* Multibus is a trademark of Intel Corporation.

Signal Processing

The capability to manipulate information in the form of discrete charge packets makes CCD technology ideal for analog signal processing. Fairchild signal processing components are monolithic silicon structures comprised of CCD analog shift registers, charge injection ports, and output charge-sensing amplifiers. They can be advantageously used for delay and temporary storage of analog video signals. The time delay for data transit through the CCD register is precisely controlled by the frequency of the externally supplied transport clock signal. Fairchild signal processing components include a sample-and-hold signal output stage for ease of application.

Fairchild video delay modules are printed circuit board structures which include the CCD321A3 device and are sold as fully assembled and calibrated units. The module is equipped for use as a variable delay circuit, using either an externally supplied or internal variable frequency clock, or for temporary analog data storage in a stopped-clock mode.

Typical applications for the CCD signal processing components and modules include time base correction for video tape recorders, fast input-slow output data expansion systems for A-D converter systems, comb filter realizations, drop-out compensators, and other analog applications up to frequencies of 30 MHz data rate.

Signal Processing Products

Order Code	Description
CCD321A1	NTSC Broadcast Quality Video Delay Line
CCD321A2	NTSC Industrial Quality Video Delay Line
CCD321A3	NTSC Time Base Correction Video Delay Line
CCD321VM	Video Delay Module (includes the CCD321A3)
CCD323A	PAL Video Delay Line

For further information on Fairchild CCD Imaging and Signal Processing products, call your nearest Fairchild Sales Office, representative, or distributor.

For technical or applications information and assistance, call (415) 493-8001, (TWX 910-373-2110) or write Fairchild CCD Imaging, 3440 Hillview Avenue, Palo Alto, California 94304.

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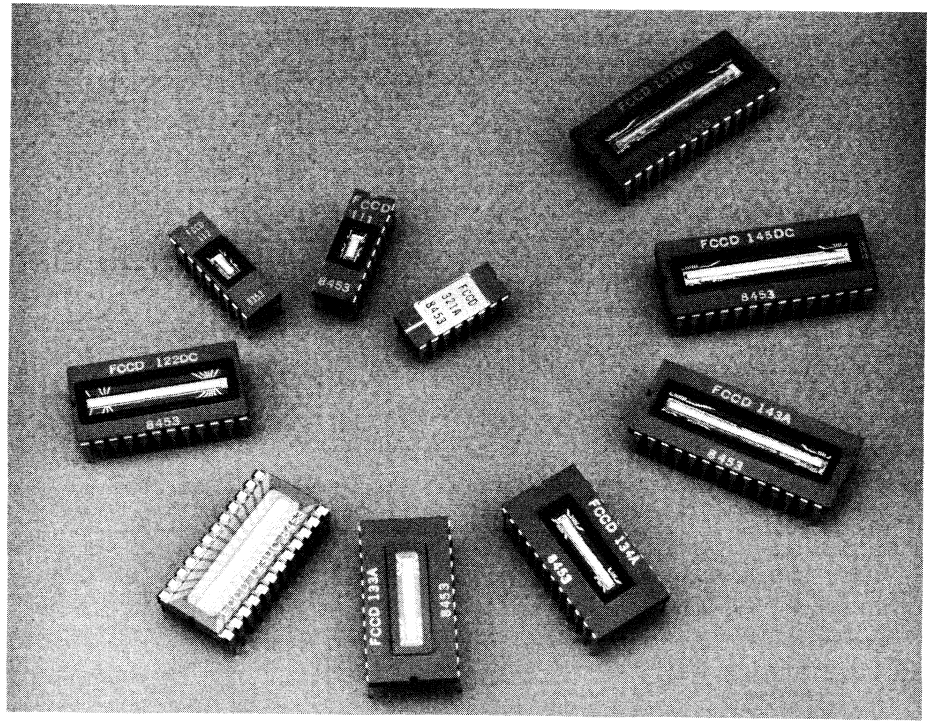

Sensors

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CCD 111
256-Element
Line Scan Image Sensor

CCD Imaging

Description

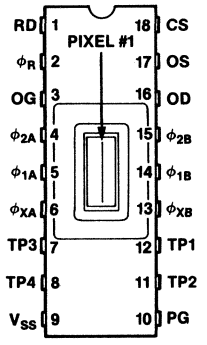
The CCD111 is a monolithic 256-element line image sensor. The device is designed for optical character recognition and other imaging applications that require high sensitivity and high speed. The CCD111 is pin-for-pin compatible with and a functional replacement for the CCD110F.

In addition to a line of 256 sensing elements, the CCD111 chip includes: two charge transfer gates, two 2-phase analog transport shift registers, an output charge detector/amplifier, and a compensation amplifier. The transport registers both feed the input of the charge detector resulting in sequential reading of the 256 sensing elements.

The cell size is 13 μm (0.51 mils) by 17 μm (0.67 mils) on 13 μm (0.51 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel isoplanar buried-channel technology.

- **DYNAMIC RANGE TYPICAL: 2500:1**
- **ON-CHIP VIDEO AND COMPENSATION AMPLIFIERS**
- **LOW POWER REQUIREMENTS**
- **ALL OPERATING VOLTAGES 15V AND UNDER**
- **LOW NOISE EQUIVALENT EXPOSURE**
- **DIMENSIONALLY PRECISE PHOTOSITE SPACING**

Connection Diagram

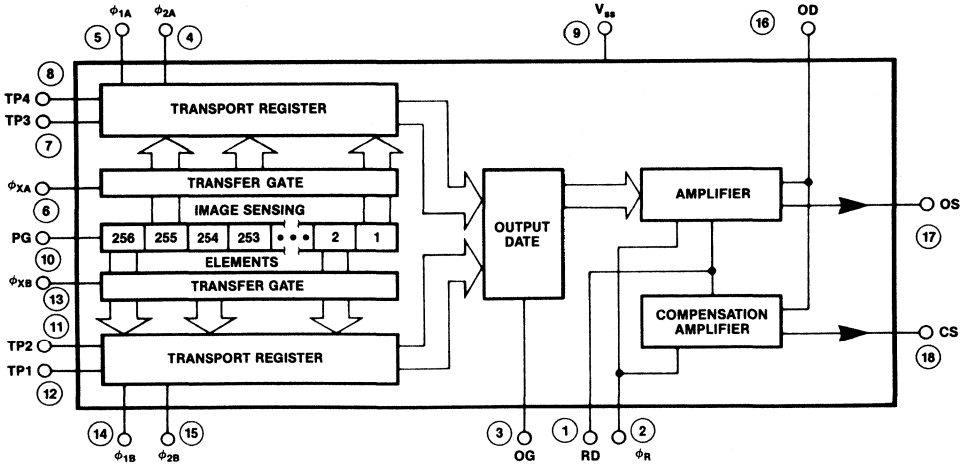


DIP (TOP VIEW)

Pin Names:

PG	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Clock
ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}	Transport Clocks
OG	Output Gate
OS	Output Source
OD	Output Drain
CS	Compensation Source
ϕ_R	Reset Clock
RD	Reset Drain
TP	Test Point
V_{SS}	Substrate (ground)

Block Diagram



Functional Description
The CCD111 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 256 image sensor elements separated by a diffused channel stop and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the left and right transport registers. The transfer gates also control the integration time for the sensing elements.

Two 130-Bit Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output OS. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Definition of Terms

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Gated Charge Detector/Amplifier — The output circuit of the CCD111 that receives the charge packets from the transport registers and provides a signal voltage proportional to the size of each charge packet received. Before each new charge packet is sensed, a reset clock returns the charge detector voltage to a fixed level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. (This does not take into account dark signal components.) Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive

CCD111

element under uniform illumination. Measurement of PRNU excludes first and last elements. (See accompanying photos for details of definition.)

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation ouput voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — A picture element (photosite).

Peripheral Response — The output signal caused by light-generated charge that is collected by the transport registers (instead of the photosites). The device is covered, except over the photosites, by a gapped metal layer, which functions both as an array of interconnections and as a reflective light shield. The major component of Peripheral Response for visible light ($\lambda \leq 700$nm) is generated in the transport registers by light transmitted through these gaps in the metal above the registers. For near-infrared light ($\lambda \geq 700$nm), especially on CCD111A devices, a portion of the charge generated by light absorbed under the photosites and one transport register is collected in the opposite transport register.

Major Differences Between the CCD111A and CCD111B
Both the CCD111A and the CCD111B have the same responsivity to visible light (400-700nm). The principal differences are as follows:

The CCD111A is intended for use in applications where very low dark signal and high responsivity to very near-infrared (700-900nm) light are needed, and where peripheral response is not critical.

The CCD111B is selected for use in applications where standard responsivity to very near-infrared (700-900nm) light and standard dark signal are acceptable and where peripheral response needs to be minimized.

It is not recommended that either part be used with illumination containing wavelengths greater than 900nm (near-infrared). If use of such a light source (unfiltered tungsten, for example) is unavoidable, the CCD111B will generally provide the user with more satisfactory results. The table on performance characteristics provides more information.

Absolute Maximum Ratings

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15	−0.3V to 15V
Pins 1, 8, 11, 16	−0.3V to 18V
Pins 17, 18	output, no voltage applied
Pin 9	OV

Caution Note
This device has limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins OS and CS to V_{SS} or V_{OD} during operation of the device. Shorting these pins temporarily to V_{SS} or V_{OD} may destroy the output amplifiers.

DC Characteristics: T_c = 25°C (Note 1)

Symbol	Characteristic	Limits Min	Limits Typ	Limits Max	Unit	Condition
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	11.5	12.0	12.5	V	
V_{OG}	Output Gate Voltage		5.0		V	
V_{PG}	Photogate Voltage	9.5	10.0	12.5	V	
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

Clock Characteristics: T_c = 25°C (Note 1)

Symbol	Characteristic	Limits			Unit	Condition
		Min	Typ	Max		
$V_{\phi 1AL}$, $V_{\phi 1BL}$ $V_{\phi 2AL}$, $V_{\phi 2BL}$	Transport Clocks LOW	0.0	0.5	0.8	V	Note 2
$V_{\phi 1AH}$, $V_{\phi 1BH}$ $V_{\phi 2AH}$, $V_{\phi 2BH}$	Transport Clocks HIGH	7.5	8.0	8.5	V	Note 5
$V_{\phi XAL}$, $V_{\phi XBL}$	Transfer Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V_{\phi XAH}$, $V_{\phi XBH}$	Transfer Clock HIGH	7.5	8.0	8.5	V	Note 5
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V_{\phi RH}$	Reset Clock HIGH	7.5	8.0	8.5	V	Notes 3, 5
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Maximum Transport Clock Frequency		5.0		MHz	Note 5
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Data Rate)		10.0		MHz	Note 6

AC Characteristics: T_c = 25°C, $f_{\phi R}$ = 1.0 MHz, t_{int} = 320 μs, $t_{transport}$ = 259 μs, Light Source = 2854°K + filters as specified. All operating voltages nominal specified values. (Note 1)

Symbol	Parameter	Range			Unit	Condition
		Min	Typ	Max		
DR	Dynamic Range (relative to rms noise) (relative to peak-to-peak noise)	 1250:1 250:1	 2500:1 500:1			Note 7
NEE	RMS Noise Equivalent Exposure		 2×10^{-4}		 $\mu J/cm^2$	
SE	Saturation Exposure		0.5		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency		99.995		%	Note 8
SR	Spectral Response Range Limits		 0.45 – 1.05		 μm	
P	Power Dissipation		100		mW	V_{OD} = 15V
Z	Output Impedance		1000		Ω	
N	RMS Noise Peak-to-Peak Noise		80 400		μV	

CCD111

Performance Characteristics: T_c = 25°C, $f_{\phi R}$ = 1.0 MHz, t_{int} = 320μs, $t_{transport}$ = 259μs, Light Source = 2854°K + filters as specified. All operating voltages nominal specified values. (Note 1)

Symbol	Characteristic	Range CCD111A Min	CCD111A Typ	CCD111A Max	CCD111B Min	CCD111B Typ	CCD111B Max	Unit	Condition
PRNU	Photoresponse Non-uniformity Peak-to-Peak								
	2854°K + 700 nm cutoff filter		35	70		25	70	mV	14, 15, 16
	2854°K + 900 nm cutoff filter		45	110		45	110	mV	14, 15, 16
	2854°K unfiltered		70			60		mV	14, 15, 16
	Single-pixel Positive Pulses		<10			<10		mV	15, 16
	Single-pixel Negative Pulses		20	60		20	60	mV	15, 16
RI	Register Imbalance ('Odd'/'Even')		<5			<5		mV	15, 16
DS	Dark Signal DC Component	0	<1	3	0	2	15	mV	2, 9, 10
	Low Frequency Component	0	<1	2	0	2	10	mV	2, 9, 11
SPDSNU	Single-pixel DS Non-uniformity	0	<1	2	0	1	2	mV	9, 11, 12
PR	Peripheral Response								
	2854°K + 700 nm cutoff filter		10	17		<2	5	% of V_{OUT}	14
	2854°K + 900 nm cutoff filter		12	20		3	7	% of V_{OUT}	14
	2854°K unfiltered		25			4		% of V_{OUT}	14
R	Responsivity								
	2854°K + 700 nm cutoff filter	0.7	1.3	2.1	0.5	1.1	2.0	V/μJ/cm²	13, 14
	2854°K + 900 nm cutoff filter	1.3	2.4	3.9	0.8	1.6	2.4	V/μJ/cm²	13, 14
	2854°K unfiltered		2.0			0.9		V/μJ/cm²	13, 14
V_{SAT}	Saturation Output Voltage	500	900		500	900		mV	17

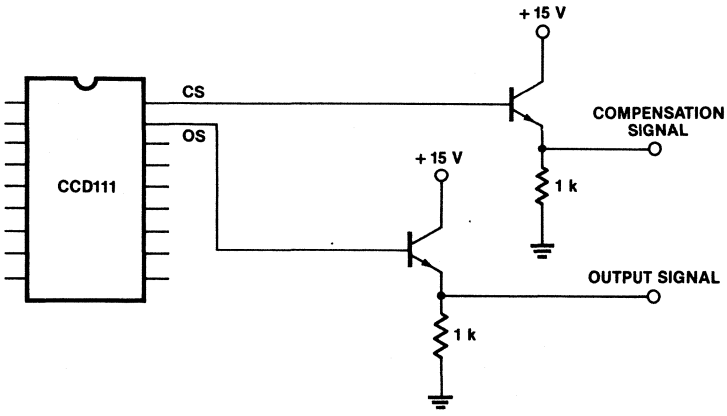
Notes

1. T_C is defined as the package temperature, measured on the back surface of the ceramic body.
2. Negative transients on any clock pin going below 0.0V may cause charge injection that results in an increase in the apparent Dark Signal.
3. $V_{\phi RH}$ should track V_{RD}.
4. The data output frequency $f_{\phi R}$ is twice that of each transport clock ($f_{\phi 1A}$, $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$).
5. $C_{\phi XA} \simeq C_{\phi XB} \simeq 20pF$, $C_{\phi 1A} \simeq C_{\phi 2A} \simeq C_{\phi 1B} \simeq C_{\phi 2B} \simeq 32pF$, $C_{\phi R} \simeq 5pF$.
6. Minimum reset clock frequency is limited by the increase in Dark Signal.
7. Dynamic Range is defined as "V_{SAT}/rms (temporal) Noise" or "V_{SAT}/Peak-to-Peak (temporal) Noise."
8. CTE is measured for a one-stage transfer.
9. See photographs for Dark Signal definitions.
10. DC and low-frequency Dark Signal components approximately double for every 5°C increase in T_C. The shift register component is also inversely proportional to $f_{\phi R}$.
11. Single-pixel Dark Signal non-uniformity (SPDSNU) approximately doubles for every 8°C increase in T_C. They are also directly proportional to the integration time t_{int}.
12. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU.
13. RESPONSIVITY is defined as the "volts of video output" per "Incident Radiant Energy measured over the 350 nm–1200 nm band." The device will not respond to infrared wavelengths longer than ≈ 1200 nm. However, 2/3 of the radiant energy from a 2854°K source is at $\lambda > 1200$ nm. For the unfiltered 2854°K source, the responsivity values for light measured over $0 < \lambda < \infty$ will be ~0.3X of the responsivity values for light measured over 350 nm $< \lambda <$ 1200 nm.

Notes (cont'd)

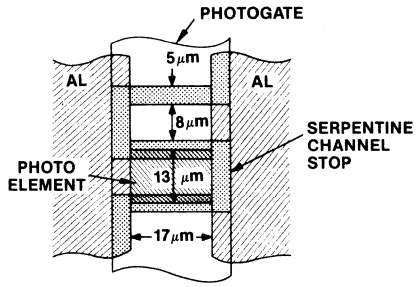
14. OPTICAL FILTERS: a "700 nm cutoff" filter is realized by using one "Wide Band Hot Mirror" (Optical Coating Labs, Inc., Santa Rosa, California) and one 2.0 mm thick "BG-38" blue glass (Schott Optical Glass, Duryea, Pennsylvania) filter in series. The "900 nm cutoff" filter is available on special order; consult Fairchild CCD Applications Engineering for details. Transmittance curves for the two cutoff filters and Spectral Energy Distribution curves for these filters with a 2854°K light source are given in the "Typical Performance Curves" section of this data sheet. It should be noted that the "2854°K + 700 nm cutoff" source is a good approximation to a Daylight Fluorescent bulb.
15. All PRNU measurements taken at a 350mV output level using a F/5.0 lens; all PRNU measurements exclude the outputs from the first and last photoelements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As f number increases, the resulting more highly collimated light causes package window aberrations to dominate and increase the PRNU. A lower f number ($f \leq 5$) results in less collimated light, causing photosite blemishes to dominate PRNU.
16. See photographs for PRNU definitions.
17. See test load configuration.

Test Load Configuration



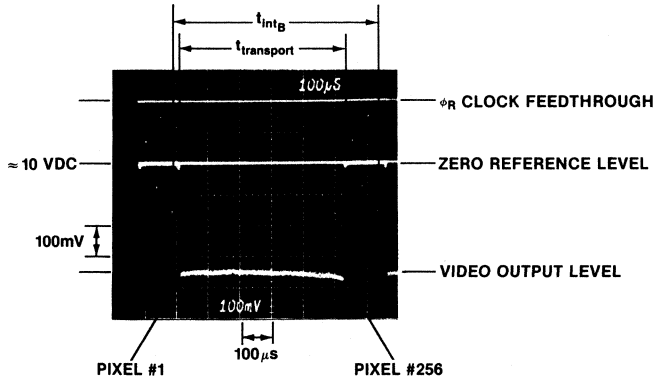
CCD111

Photoelement Dimensions



ALL DIMENSIONS ARE TYPICAL VALUES.

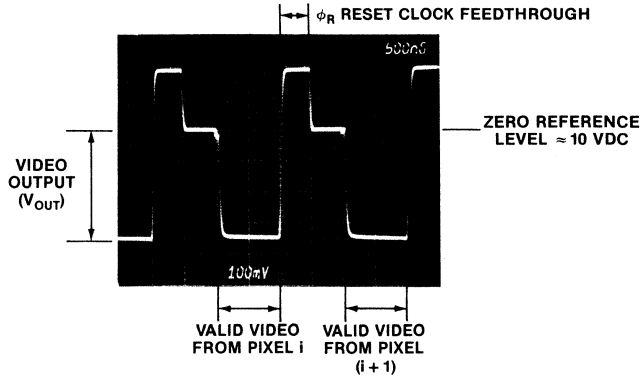
Output with Uniform Illumination



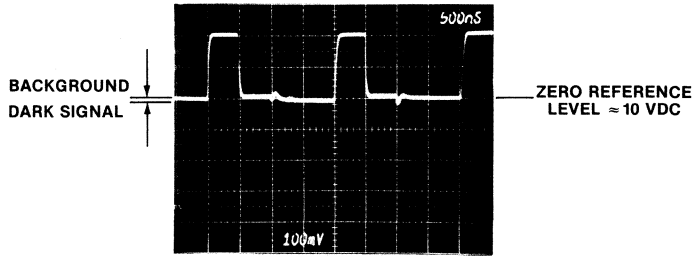
TEST CONDITIONS: T_C = +25°C, t_{int} = 640 μs, $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

Output of Two Pixels

DEVICE ILLUMINATED



DEVICE IN DARK

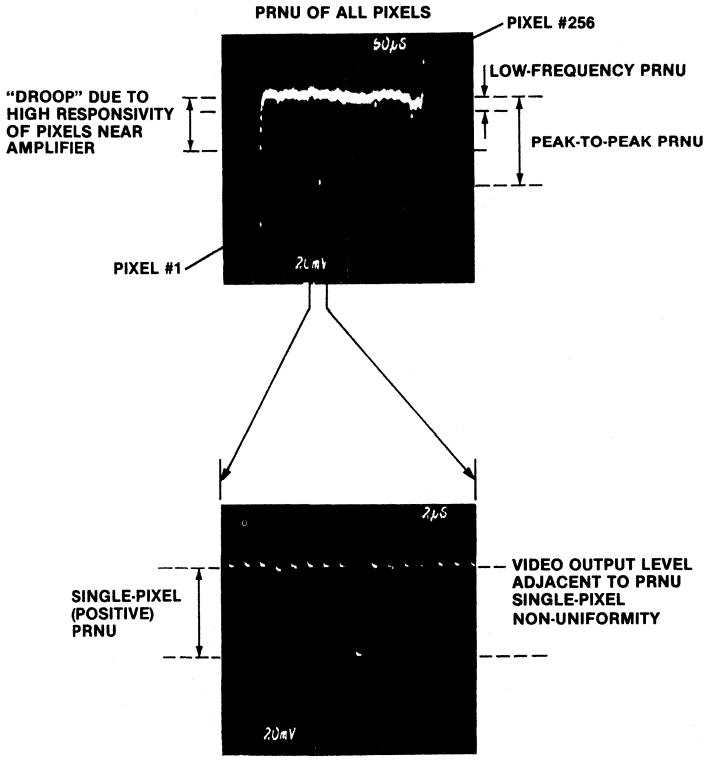


TEST CONDITIONS: T_C = +25°C, t_{int} = 640 μs, $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

CCD111

Photoresponse Non-uniformity

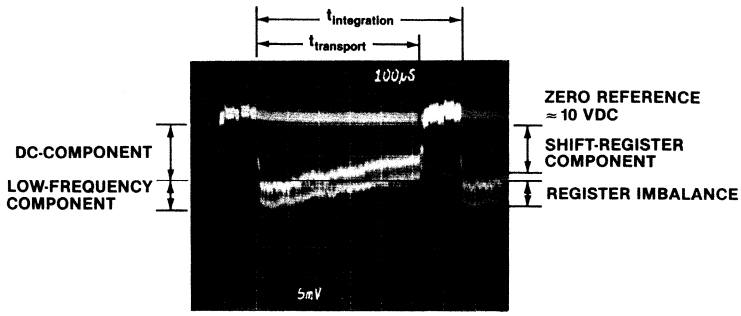
MEASURED AT V_{OUT} = 350 mV; ALL PRNU COMPONENTS EXCLUDE PIXELS #1 AND #256.



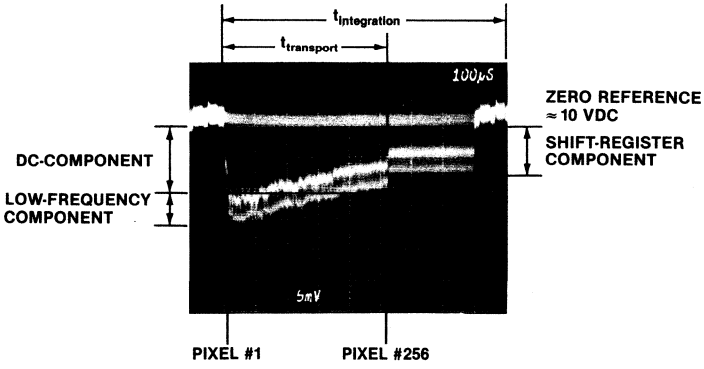
TEST CONDITIONS: T_C + 25°C, t_{int} = 320 μs, $f_{\phi R}$ = 1.0 MHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set.

DC + Low Frequency Dark Signal

AT t_{int} = 640μs:



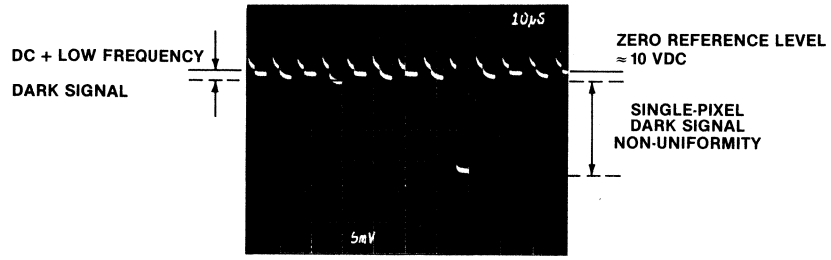
AT t_{int} = 900μs, OTHER INPUTS SAME AS ABOVE:



TEST CONDITIONS: T_C = +25°C, t_{int} = (see above), f_{dR} = 512 kHz, "typ" voltage inputs. (Half standard test speeds for clearer photos.)

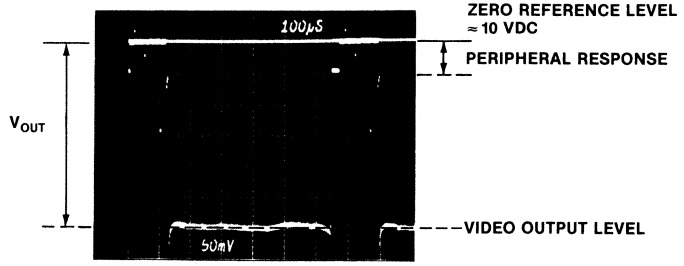
CCD111

Single-pixel Dark Signal Non-uniformity



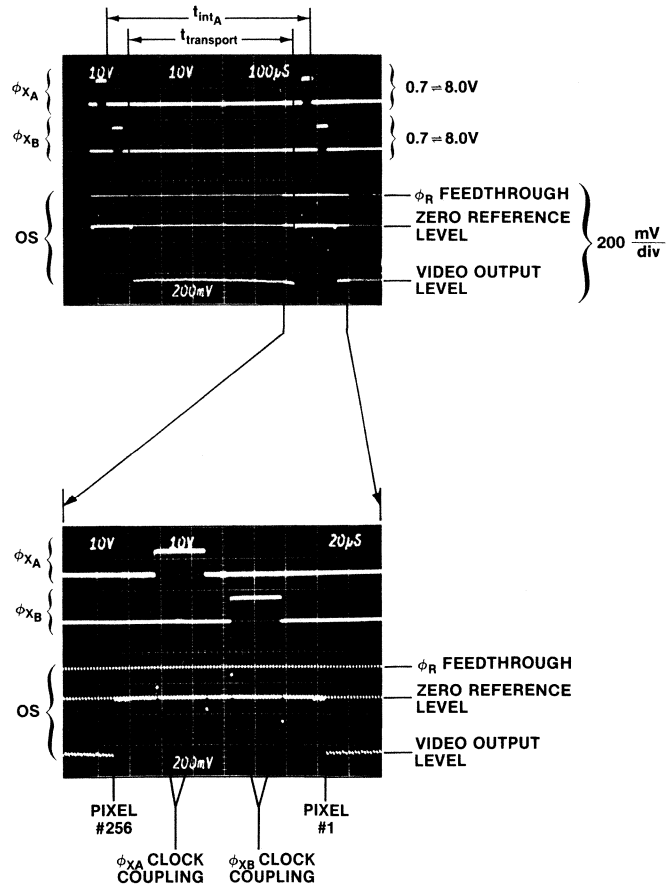
TEST CONDITIONS: T_C = +25°C, t_{int} = 2.560 ms, $f_{\phi R}$ = 128 kHz, "typ" voltage inputs. (One-eighth standard test speeds to emphasize Dark Signal.)

Peripheral Response



TEST CONDITIONS: T_C = +25°C, t_{int} = 640 μs, $f_{\phi R}$ = 510 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

ϕ_X(Transfer Clock) Coupling into OS (Output)



TEST CONDITIONS: T_C = +25°C, T_{int} = 640 μs, $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

CCD111

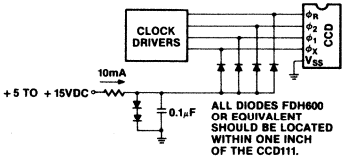
Device Care and Operation

Charge Injection: Every input pin has a gate protection structure that includes a diode from the input to the (grounded) substrate V_{SS}. The diode is reverse-biased during normal operation ($V_{in} > V_{SS}$). Negative (transient) input voltages ($V_{in} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chip.

If sufficient charge is injected, it will accumulate in the transport register(s) and/or the photosites near the injecting gate protection structure(s). Injected charge which accumulates in the photosites will typically result in an apparent bell-shaped increase in Dark Signal (≈ 20-200 pixels wide) near the injecting gate protection structure. Injected charge which accumulates in a transport register will result in an apparent uniform increase in that register's low frequency dark signal, creating a noticeable increase in the apparent Register Imbalance ("odd/even") of the Dark Signal.

The susceptibility to charge injection sufficient to increase the DC and Low Frequency Dark Signal varies significantly from device to device. It is not possible to select devices with "low" susceptibility. However, devices with low Dark Signal are typically more susceptible than devices with high Dark Signal.

Sufficient charge to appear as increased DC and Low Frequency Dark Signal may be injected by negative transient voltages <4 ns long. Since these transients cannot be detected by oscilloscopes with less than 250-500 MHz bandwidth, a system which appears to be free from negative transients on a 200 MHz scope may still be prone to charge injection. The recommended method to eliminate charge injection is the following diode clipper circuit:

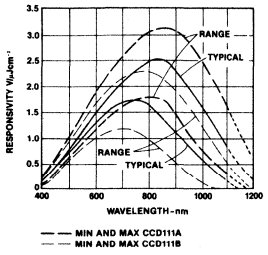


It is also important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The DC and Low Frequency Dark Signal approximately doubles for every 5°C temperature increase and Dark Signal Non-Uniformities approximately double for every 8°C increase. The devices may be cooled to achieve very long integration times and very low light level capability.

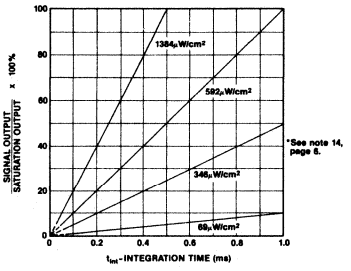
Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

Typical Performance Curves

TYPICAL SPECTRAL RESPONSE

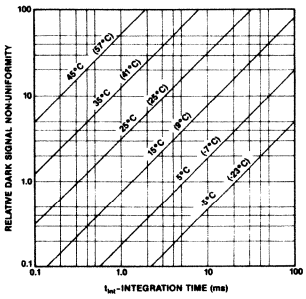


OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTER*



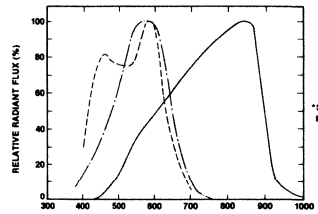
Typical Performance Curves (cont'd)

DARK SIGNAL NON-UNIFORMITY
VERSUS INTEGRATION TIME



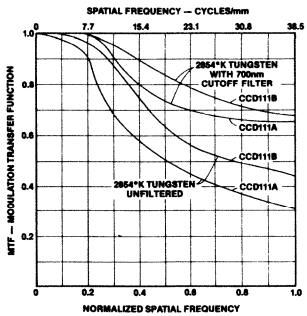
NOTE:
DC and low-frequency dark signal temperature in **bold** and SPDSNU in (parenthesis).

RELATIVE RADIANT FLUX
VERSUS WAVELENGTH*

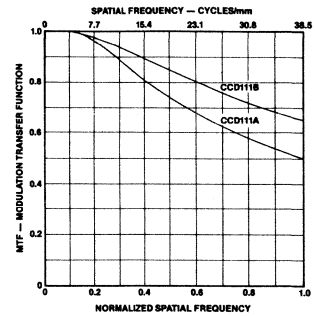


*See note 14, page 8.

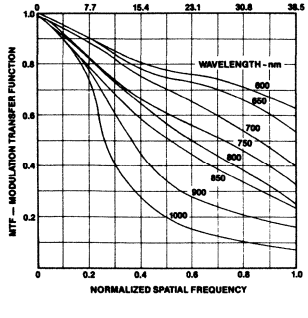
MODULATION TRANSFER FUNCTIONS
FOR TWO BROADBAND
ILLUMINATION SOURCES



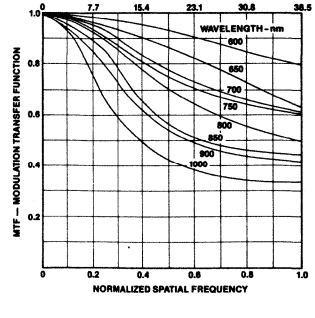
MODULATION TRANSFER FUNCTIONS
FOR A 500nm–900nm BANDPASS
ILLUMINATION SOURCES



CCD111A MODULATION
TRANSFER FUNCTIONS FOR
NARROW BAND ILLUMINATION SOURCES

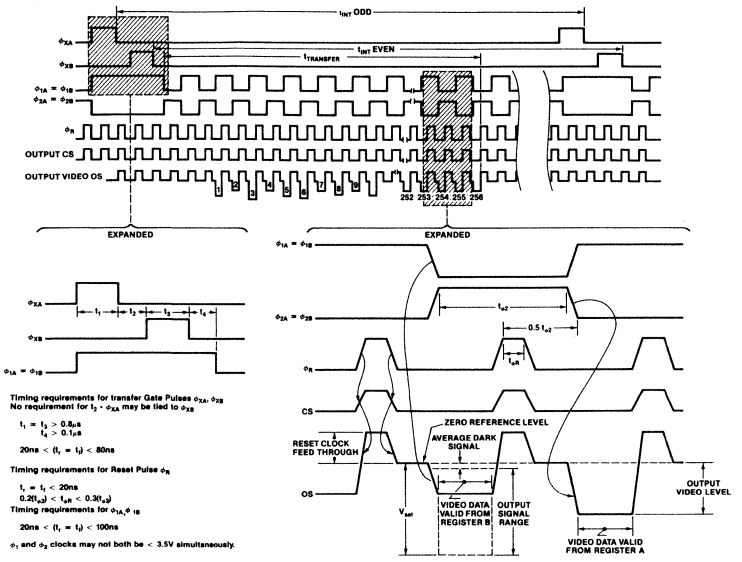


CCD111B MODULATION
TRANSFER FUNCTIONS FOR
NARROW BAND ILLUMINATION SOURCES



CCD111

Timing Diagram Drive Signals



Timing requirements for transfer Gate Pulses ϕ_{XA}, ϕ_{XB}
No requirement for t_2 - ϕ_{XA} may be tied to ϕ_{XB}

$t_1 = t_3 > 0.8\mu s$
$t_4 > 0.1\mu s$

$20ns < (t_r = t_f) < 80ns$

Timing requirements for Reset Pulse ϕ_R

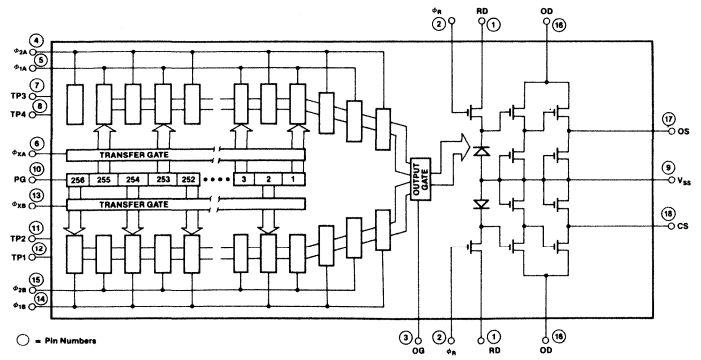
$t_r = t_f < 20ns$
$0.2(t_{x2}) < t_{xR} < 0.3(t_{x2})$

Timing requirements for ϕ_{1A},ϕ_{1B}

$20ns < (t_r = t_f) < 100ns$

ϕ_1 and ϕ_2 clocks may not both be < 3.5V simultaneously.

Circuit Diagram



○ = Pin Numbers

Order Information
It is important to note that two different selections of the CCD111 are being offered for applications that differ in the wavelength of light used for imaging. Please refer to the section "Major Differences Between the CCD111A and CCD111B" on page 3 before placing an order.

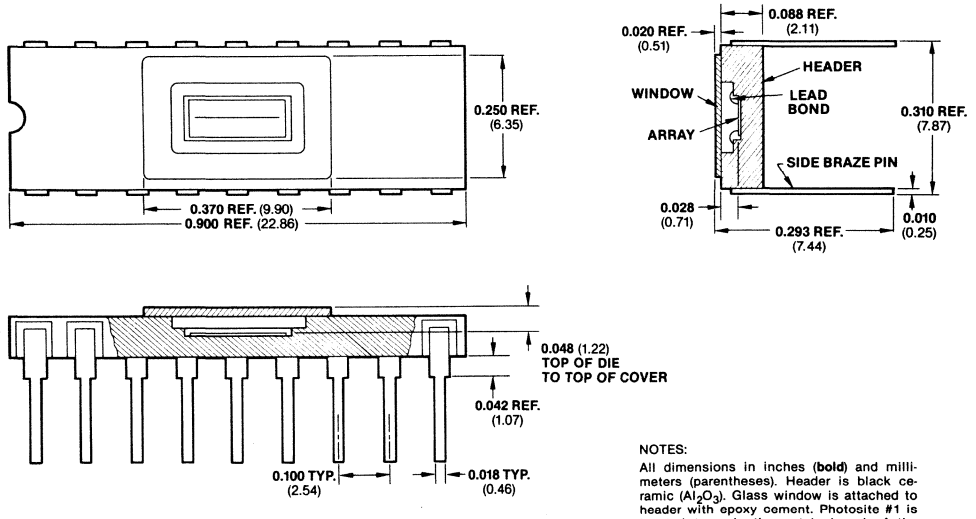
To order the CCD111, please follow the ordering codes listed in the table below:

Description	Device Type Order Code
CCD111A 256 x 1 Line Image Sensor	CD111ADC
CCD111B 256 x 1 Line Image Sensor	CD111BDC

A printed circuit board is available which includes all the necessary clocks, logic drivers, and video amplifiers to operate the CCD111. The board is fully assembled and tested and requires ± 15V and + 5V supplies for operation. The printed circuit board order code is: CCD111DB.

For further information on the boards, please call your nearest Fairchild Sales Office. For technical assistance, call (415) 493-8001.

CCD111DC Package Outline
18-Pin Dual In-Line Ceramic Package



NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement. Photosite #1 is located towards the notched end of the package. Terminal #9 is electronically connected to the Substrate (V_{SS}).

FAIRCHILD
A Schlumberger Company

CCD

I-SCAN

DESIGN DEVELOPMENT SET

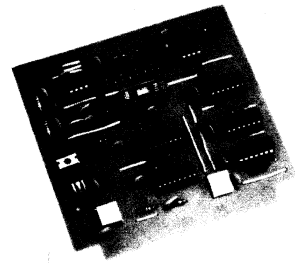
The I-SCAN design development set is being specially offered by Fairchild as a low cost tool with which to gain understanding of charge-coupled devices principles. The set includes a Fairchild CCD111, 256 element line scan sensor, mounted on a printed circuit card that contains all the necessary CCD111 operating electronics.

I-SCAN is intended for use as a construction aid for experimental systems using CCD line scan sensors or can be incorporated directly into systems requiring 256 elements of resolution.

I-SCAN comes fully assembled and tested and requires only the input of power supplies and an oscilloscope to display the video information corresponding to the image placed in front of the sensor.

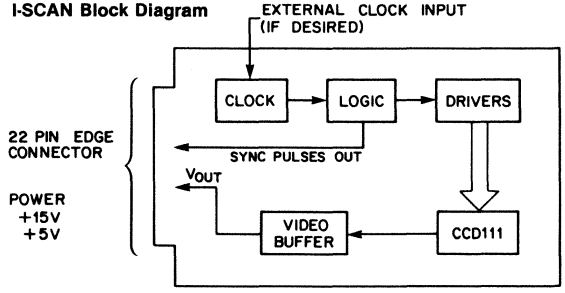
The I-SCAN printed circuit card (block diagram) includes a variable frequency clock generator that can be overriden by an external input, logic circuitry for timing the drive signals, drivers to interface the TTL logic to CCD levels and video buffer circuits.

Detailed schematics, a parts layout drawing and timing diagram are included with I-SCAN.



To operate the board, supply +5V and +15V through a 22-pin standard edge connector to the PC board. Video information as well as synchronization pulses are supplied to the connector for display on an oscilloscope.

I-SCAN Block Diagram



To order I-SCAN, follow the order code below:

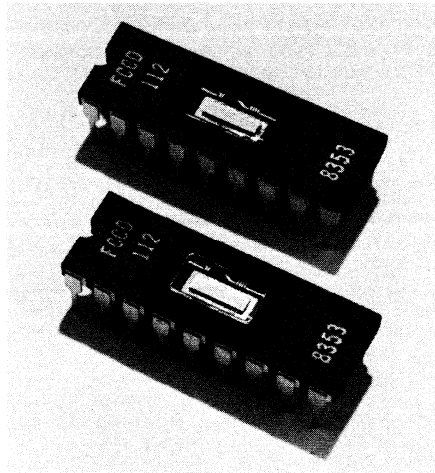
Description	Order Code
I-SCAN 256-Element Line Scan Design Development Set	I-SCAN

CCD Imaging
"Sensing the Future"

CCD112
256-Element
Line Scan Image Sensor

Preliminary

CCD Imaging



DESCRIPTION

The CCD112 is a monolithic 256-element line image sensor. The device is designed for optical character recognition and other imaging applications that require high sensitivity and high speed.

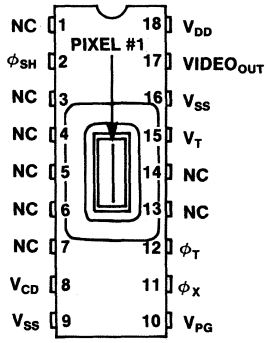
The CCD112 has overall improved performance compared with the CCD111 including higher sensitivity, an enhanced blue response and a lower dark signal. The devices also incorporate on-chip clock driver circuitry.

The photoelement size is 13μm (0.51 mils) by 13μm (0.51 mils) on 13μm (0.51 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

FEATURES

- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1V PEAK-TO-PEAK OUTPUTS**
- **DARK REFERENCE CONTAINED IN A SAMPLED-AND-HELD OUTPUT**
- **SINGLE POWER SUPPLY**

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

V_{PG}	Photogate
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
$VIDEO_{OUT}$	Output Amplifier Source
V_{DD}	Output Amplifier Drain
V_{CD}	Clock Driver Drain
V_T	Analog Transport Shift Registers DC Electrode
ϕ_{SH}	Sample-and-Hold Gate
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

FAIRCHILD
A Schlumberger Company

CCD

CCD122/142

The CCD142 is no longer carried. It has been replaced by the CCD143.

1728/2048-ELEMENT LINEAR IMAGE SENSOR

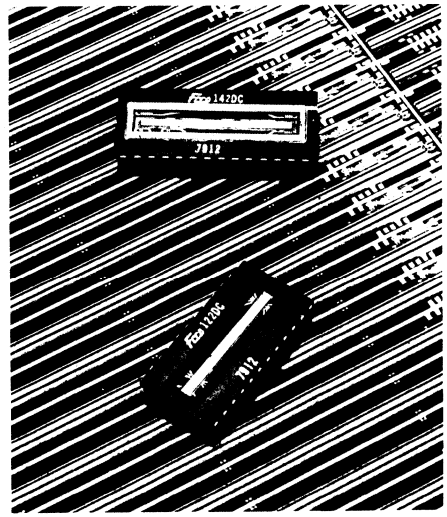
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION—The CCD122 and CCD142 are monolithic 1728 and 2048-element line image sensors, respectively. The devices are designed for page scanning applications including facsimile, optical character recognition and other imaging applications which require high resolution and high sensitivity.

The 1728 sensing elements of the CCD122 provide a 200-line per inch resolution across an 8-1/2 inch page adopted as an international facsimile standard. The 2048 sensing elements of the CCD142 provide an 8-line per millimeter resolution across a 256 millimeter page adopted as the Japanese facsimile standard.

The CCD122 and the CCD142 have overall improved performance compared with the CCD121H including higher sensitivity, an enhanced blue response and a lower dark signal. The devices also incorporate on-chip clock driver circuitry.

The photoelement size is 13 μ (0.51 mils) by 13 μ (0.51 mils) on 13 μ (0.51 mils) centers. The devices are manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.



- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1V PEAK-TO-PEAK OUTPUT**
- **DARK AND WHITE REFERENCES CONTAINED IN A SAMPLED-AND-HELD OUTPUT**
- **SINGLE POWER SUPPLY**

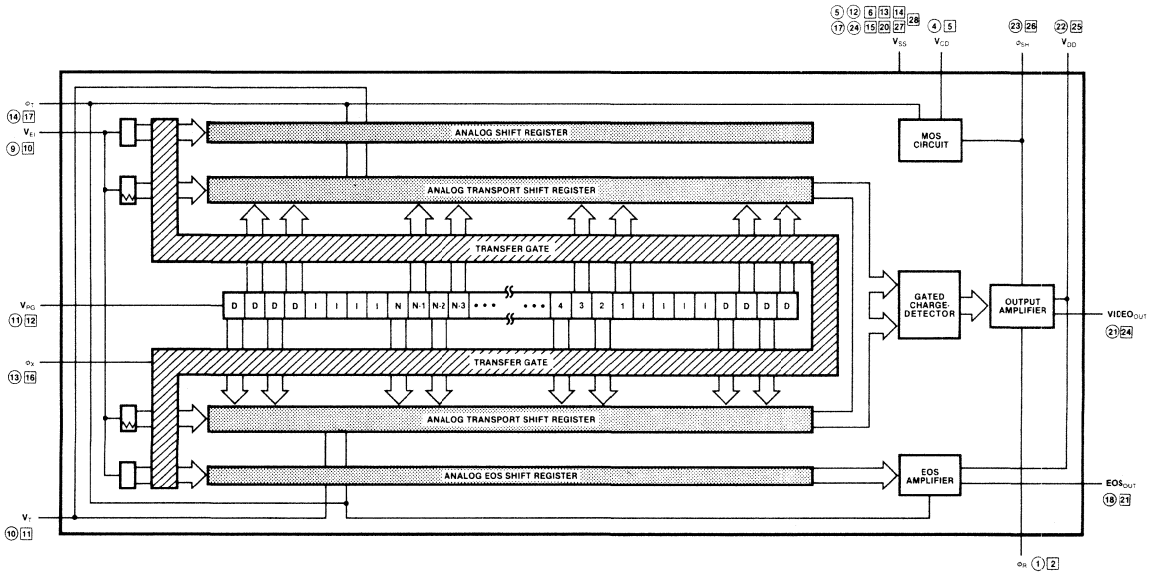
PIN NAMES

V_{PG}	Photogate
ϕX	Transfer Clock
ϕT	Transport Clock
$VIDEO_{OUT}$	Output Amplifier Source
V_{DD}	Output Amplifier Drain
ϕR	Reset Clock
V_{CD}	Clock Driver Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
EOS_{OUT}	End-of-Scan Output
ϕSH	Sample-and-Hold Clock
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

CCD122/142 VS. CCD121H COMPARISON

PARAMETER	CCD122/142	CCD121H
Spectral Response — Blue	4:1 Improvement	—
Overall	2:1 Improvement	—
Dark Signal	2:1 Improvement	—
Responsivity	2:1 Improvement	—
On-Chip Clock Drivers	Yes	No
Dark and White References	Yes	No
Single Power Supply	Yes	No

BLOCK DIAGRAM

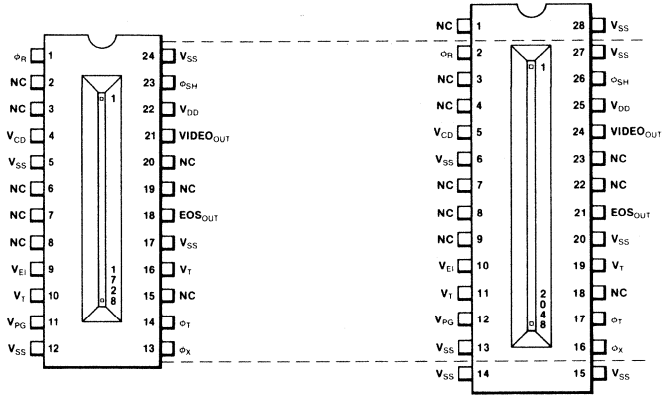


○ = CCD122 Pin Number
□ = CCD142 Pin Number
D = Dark Reference
W = White Reference
I = Isolation Cell

CCD122: N = 1728
CCD142: N = 2048

FAIRCHILD • CCD122/142

CONNECTION DIAGRAM
DIP (TOP VIEW)



CCD122 CCD142

FUNCTIONAL DESCRIPTION—The CCD122/142 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A line of 1728/2048 image sensor elements separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate — Gate structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements and permits entry of charge to the End-Of-Scan (EOS) shift registers creating the end-of-scan waveform.

Four 879/1039-Bit Analog Shift Registers — Two on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside resisters, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the charge-detector/amplifier. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of

charge-packets to establish the original serial sequence of the line of video in the output circuit. The outer two registers serve to deliver the end-of-scan waveform and reduce peripheral electron noise in the inner shift registers.

Gated Charge-Detector/Amplifer — Charge-packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sampled-and-held waveform. A reset transistor is driven by the Reset Clock (ϕ_R) and recharges the charge-detector diode capacitance before the arrival of each new signal charge-packet from the transport registers.

Clock Driver Circuitry — Allows the CCD122/142 to be operated using only three external clocks, (1) a Reset Clock signal which controls the integrated output signal amplifier, (2) a square wave Transport Clock which operates at half the reset clock frequency and controls the readout rate of video data from the sensor, and (3) a Transfer Clock pulse which controls exposure time of the sensor. The external clocks should be able to supply TTL level power.

Dark and White Reference Circuitry — Four additional sensing elements at both ends of the 1728/2048 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video ouptut representing the illuminated 1728/2048 sensor elements (labelled "D" in the block diagram). Also included at one end of the 1728/2048 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labelled "W" in the block diagram). These reference levels are useful as inputs to external DC restoration and/or automatic gain control circuitry.

DEFINITION OF TERMS:

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕ_X — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕ_T — The clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifier.

Gated Charge-Detector/Amplifier — The output circuit of the CCD122/142 which receives the charge-packets from the CCD transport shift registers and provides a signal voltage proportional to the size of each charge-packet received. Before each new charge-packet is sensed, a reset clock returns the charge-detector voltage to a fixed base level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge-detector.

Sample-and-Hold Clock ϕ_{SH} — An internally supplied voltage waveform applied to the sample-and-hold gate in the amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting ϕ_{SH} to V_{DD}.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization providing a reference voltage equivalent to device operation in the dark. Permits use of external dc restoration circuitry.

White Reference — Video output level generated by on-chip circuitry providing a reference voltage permitting external automatic gain control circuitry to be used. The reference voltage is produced by charge-injection under the control of the electrical input bias voltage (V_{EI}). The amplitude of the reference is typically 70% of the saturation output voltage.

Isolation Cell — A site on-chip producing an element in the video output that serves as a buffer between valid video data and dark and white reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the peak-to-peak noise equivalent exposure. (This does not take into account any dark signal components.) Dynamic range is

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sometimes defined in terms of rms noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

Peak-to-Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal — The output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of defintion.)

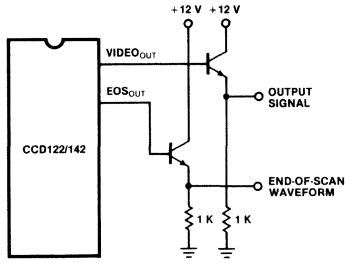
Total Photoresponse Non-Uniformity — The difference of the response levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum usable signal output voltage, measured from the zero reference level. (See timing diagram.) Any photoelement whose video output < saturation output voltage has an in-spec charge transfer efficiency (CTE). CTE will be below the specification if the video output ≥ saturation output voltage.

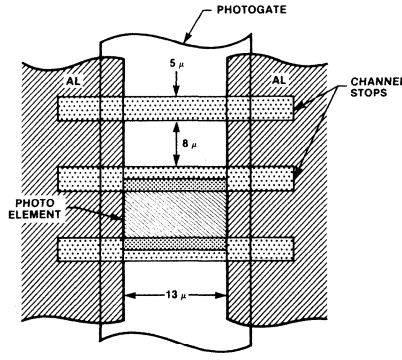
Integration Time — The time interval between the falling edges of any two successive transfer pulses ϕX as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite).

TEST LOAD CONFIGURATION



PHOTOELEMENT DIMENSIONS



All dimensions are typical values

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature		− 25 °C to + 125 °C
Operating Temperature (See curves)		− 25 °C to + 70 °C
CCD122:	Pins 1, 4, 9, 10, 11, 13, 14, 16, 22, 23	− 0.3 V to 15 V
	Pins 5, 12, 17, 24	0 V
	Pins 2, 3, 6, 7, 8, 15, 18, 19, 20, 21	NC
CCD142:	Pins 2, 5, 10, 11, 12, 16, 17, 19, 25, 26	− 0.3 V to 15 V
	Pins 6, 13, 14, 15, 20, 27, 28	0 V
	Pins 1, 3, 4, 7, 8, 9, 18, 21, 22, 23, 24	NC

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins VIDEOOUT and EOSOUT to VSS or VDD during operation of the devices. Shorting these pins temporarily to VSS or VDD may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{CD}	Clock Driver Drain Supply Voltage	12.0	13.0	14.0	V	
I_{CD}	Clock Driver Drain Supply Current		6.9	12.5	mA	
V_{DD}	Output Amplifier Drain Supply Voltage	12.0	13.0	14.0	V	
I_{DD}	Output Amplifier Drain Supply Current		6.9	12.5	mA	
V_{PG}	Photogate Bias Voltage	6.5	7.0	7.5	V	
V_T	DC Electrode Bias Boltage	4.5	5.0	5.5	V	Note 2
V_{EI}	Electrical Input Bias Voltage		11.4		V	Note 3
V_{SS}	Substrate (Ground)		0.0		V	

AC CHARACTERISTICS: (Note 1)
T_P = 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter. All operating voltages nominal specified values.

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range					
	(relative to peak-to-peak noise)	250:1	500:1			Note 9
	(relative to rms noise)	1250:1	2500:1			
NEE	RMS Noise Equivalent Exposure		0.0002		$\mu j/cm^2$	Note 10
SE	Saturation Exposure		0.4		$\mu j/cm^2$	Note 11
CTE	Charge Transfer Efficiency		0.999995			Note 12
V_O	Output DC Level	3.0	5.5	10.0	V	
Z	Output Impedance		1.4	3.0	kΩ	
P	On-Chip Power Dissipation					
	Clock Drivers		90	150	mW	
	Amplifiers		90	150	mW	
N	Peak-to-Peak Noise		2.0		mV	

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CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi TL}$	Transport Clock LOW	0.0	0.3	0.5	V	Notes 4, 5
$V_{\phi TH}$	Transport Clock HIGH	9.75	10.0	10.5	V	Note 5
$V_{\phi XL}$	Transfer Clock LOW	0.0	0.3	0.5	V	Notes 4, 6
$V_{\phi XH}$	Transfer Clock HIGH	9.75	10.0	10.5	V	Note 6
$V_{\phi RL}$	Reset Clock LOW	0.0	0.3	0.5	V	Note 7
$V_{\phi RH}$	Reset Clock HIGH	9.75	10.0	10.5	V	Note 7
$f_{\phi R}$	Maximum Reset Clock Frequency (Output Data Rate)	1.0	2.0		MHz	Note 8

PERFORMANCE CHARACTERISTICS: (Note 1)

T_P = 25°C, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, light source = 2854°K + 3.0 mm thick Corning 1-75 IR-absorbing filter. All operating voltages nominal specified values.

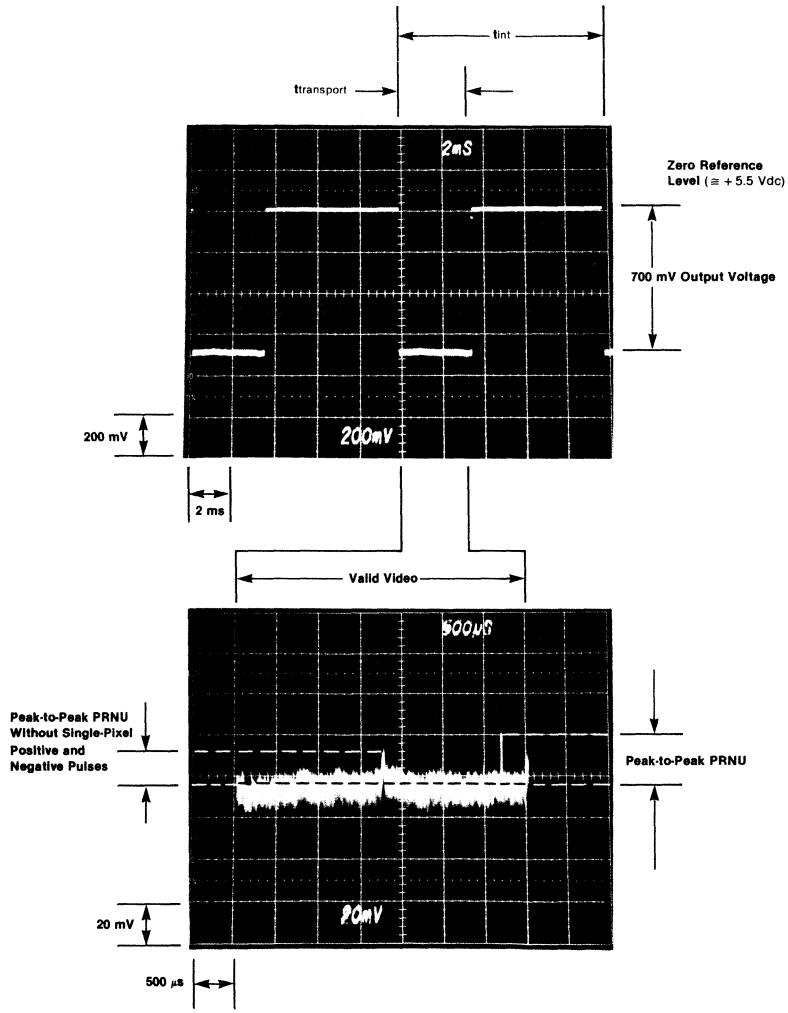
SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU*	Photoresponse Non-uniformity					
	Peak-to-Peak		160	210	mV	Note 16
	Peak-to-Peak without Single-Pixel Positive and Negative Pulses		100		mV	Note 16
	Single-pixel Positive Pulses		85		mV	Note 16
	Single-pixel Negative Pulses		130		mV	Note 16
	Register Imbalance ("Odd"/"Even")		20		mV	Note 16
DS	Dark Signal					
	DC Component		5	15	mV	Notes 13, 14
	Low Frequency Component		5	10	mV	Notes 13, 14
SPDSNU	Single-pixel DS Non-uniformity		20	40	mV	Notes 13, 15
R	Responsivity	2.0	3.5	5.0	Volts per $\mu j/cm^2$	Note 17
V_{SAT}	Saturation Output Voltage	800	1400	1600	mV	Note 18

*All PRNU Measurements taken at a 700 mV output level using an f/2.8 lens and excluded the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the f number increases, the resulting more highly columnated light causes the package window aberrations to dominate and increase PRNU. A lower f number results in less columnated light causing device photosite blemishes to dominate the PRNU.

NOTES:

1. T_P is defined as the package temperature.
2. V_T should be equal to (1/2) $V_{\phi TH}$.
3. V_{EI} is used to generate the end-of-scan output and the white reference output. These two signals can be eliminated by connecting V_{EI} to a voltage level equal to $V_{\phi XH}$ + 5 V.
4. Negative transients on any clock pin going below 0.0 V may cause charge-injection which results in an increase of apparent DS.
5. $C_{\phi T} \cong$ 700 pF
6. $C_{\phi X} \cong$ 300 pF
7. $C_{\phi R} \cong$ 5 pF
8. Minimum clock frequency is limited by increase in dark signal.
9. Dynamic range is defined as V_{SAT}/peak-to-peak (temporal) or V_{SAT}/rms noise.
10. 1 $\mu j/cm^2$ = 0.02 fcs at 2854°K, 1 fcs = 50 $\mu j/cm^2$ at 2854°K.
11. SE for 2854°K for light without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 0.8 $\mu j/cm^2$.
12. CTE is the measurement for a one-stage transfer.
13. See photographs for DS definitions.
14. Dark signal component approximately doubles for every 5°C increase in T_P.
15. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in T_P.
16. See photographs for PRNU definitions.
17. Responsivity for 2854°K light source without 3.0 mm thick Corning 1-75 IR-absorbing filter is typically 2 V per $\mu j/cm^2$.
18. See test load configurations.

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS

TP ≅ +25°C, f_{eR} = 0.5 MHz, tint = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

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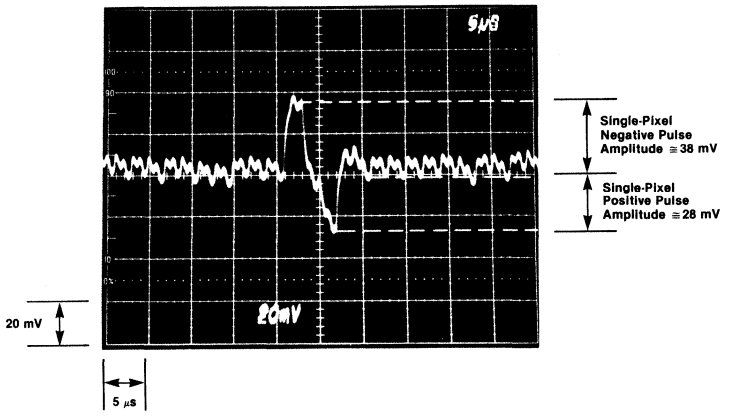
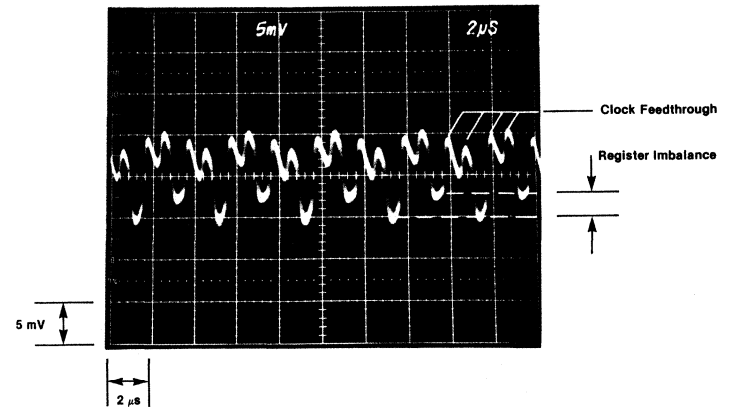
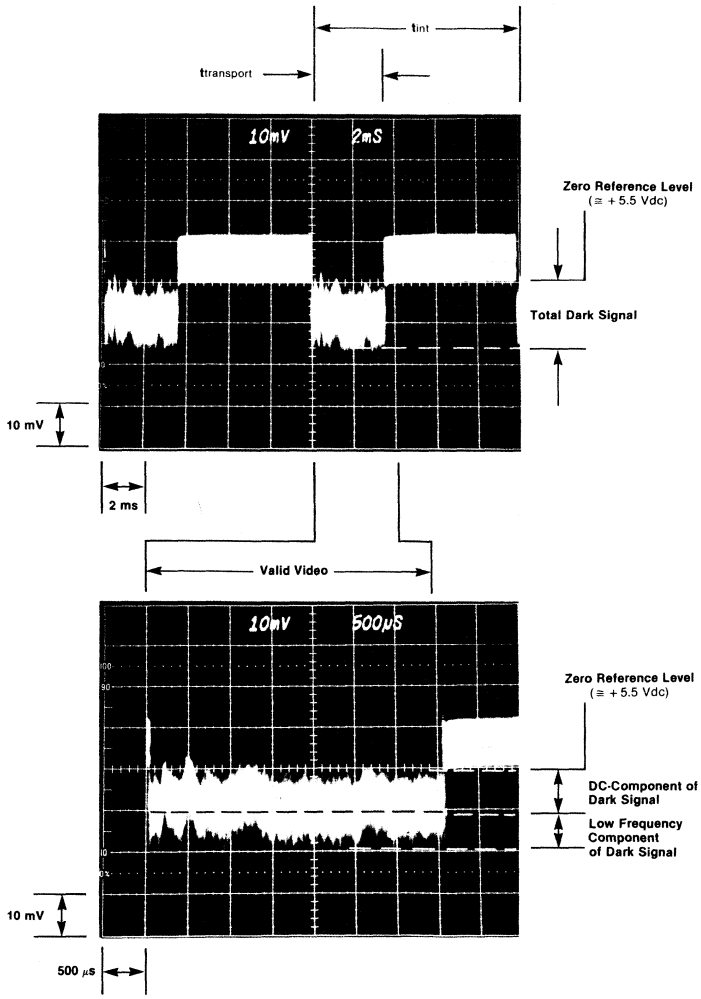
PRNU PARAMETERS (CONTINUED)





TEST CONDITIONS
$T_P \cong +25°C$, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10.0 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

DARK SIGNAL PARAMETERS (DS)



TEST CONDITIONS

TP ≅ +25°C, $f_{\phi R}$ = 0.5 MHz, tint = 10.0 ms, all voltages nominal specified values.

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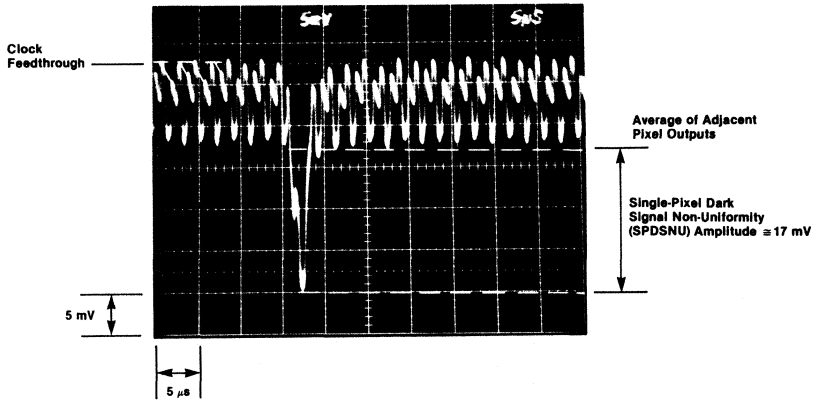
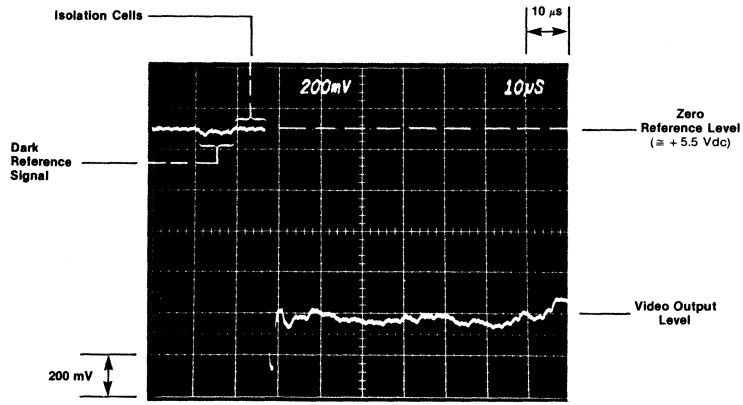
DS PARAMETERS (CONTINUED)

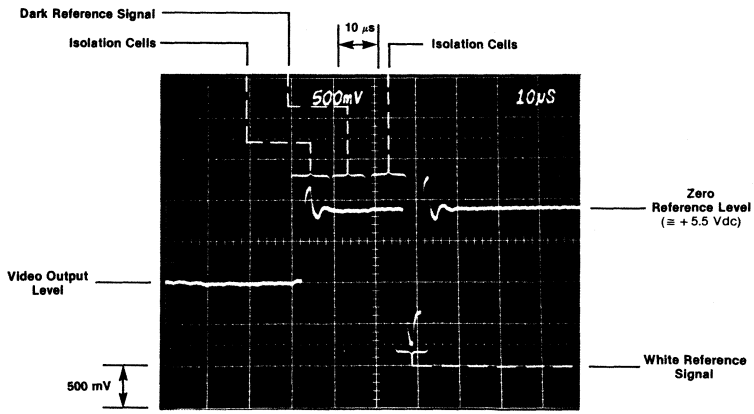


TEST CONDITIONS
TP ≅ +25°C, fφR = 0.5 MHz, tint = 10.0 ms, all voltages nominal specified values.

VIDEO OUPUT TIMING PHOTOGRAPHS



START OF ONE SCAN VIDEO OUTPUT



END OF ONE SCAN VIDEO OUTPUT

TEST CONDITIONS

$T_P \cong +25°C$, $f_{\phi R}$ = 0.5 MHz, t_{int} = 10 ms, all voltages nominal spec-sheet values. Illumination: 2854°K source with a 3.0 mm thick Corning 1-75 IR-absorbing filter. PRNU measurements taken at an output voltage of 700 mV.

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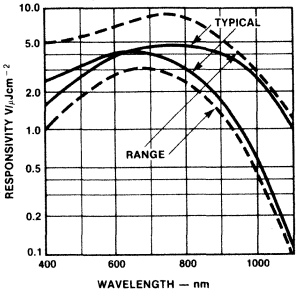
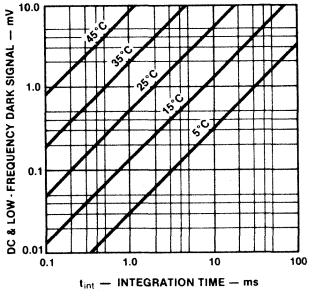
TYPICAL PERFORMANCE CURVES

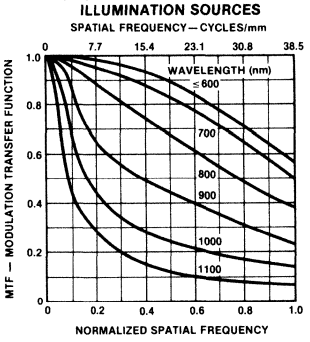
TYPICAL SPECTRAL RESPONSE



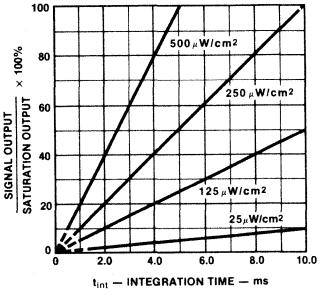
DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME



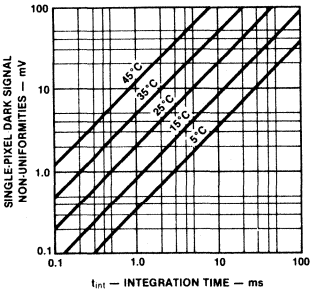
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



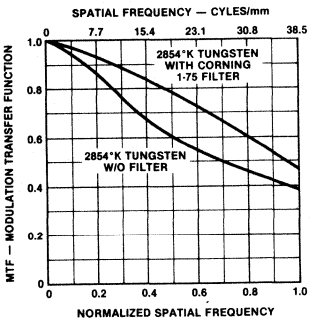
OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH CORNING 1-75 FILTER



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

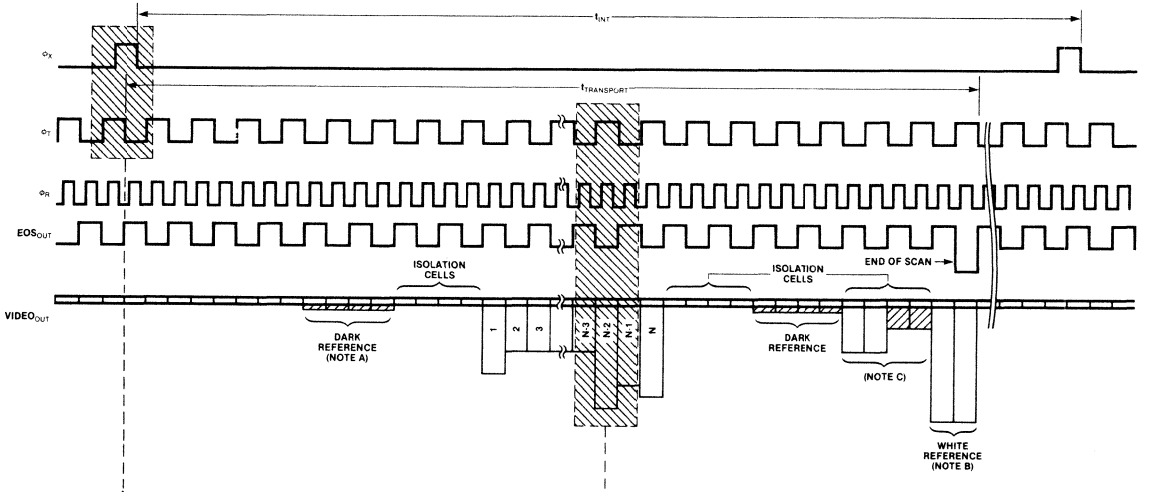


MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



The Corning 1-75 filter has the following typical transmittance spectral characteristic: >85% at <600 nm, 60% at 700 nm, 30% at 800 nm, 5% at 900 nm and <2% at >1000 nm.

TIMING DIAGRAM DRIVE SIGNALS



Timing requirements for transfer pulse ϕ_X (Note D). A ϕ_X pulse must straddle a ϕ_T transition as shown.

$t_{\phi X} > 200$ ns $\quad t_{\phi 1} > 100$ ns $\quad t_{\phi 2} > 100$ ns

Timing requirements for reset pulse ϕ_R (Note D)

$t_{\phi R} > 40$ ns $\quad t_{\phi 3} > 350$ ns $\quad t_{\phi 4} > 120$ ns

NOTES:

A. The first and last elements of the dark reference signal output may not contain a valid representation of that signal.

B. White reference cell output signals will be approximately equal in height.

C. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.

D. Recommended rise and fall times for all clocks are that they are ≥20 ns.

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DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

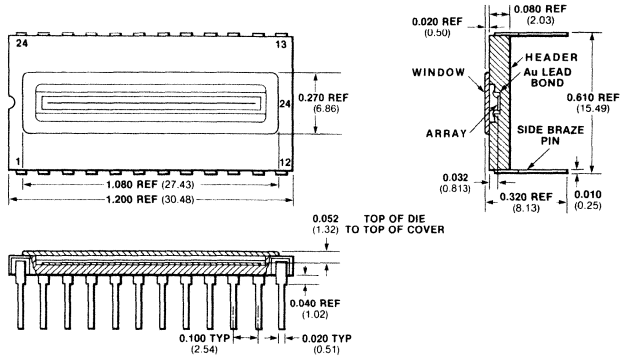
It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION — Order CCD122DC where "D" stands for a ceramic package and "C" for commercial temperature range.

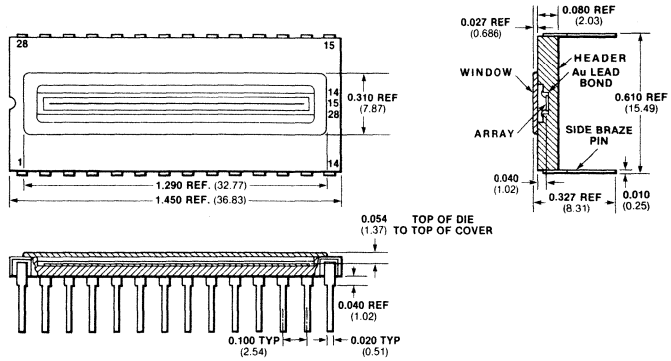
The pins on the CCD122DC and the CCD142DC are arranged to allow the 24-pin CCD122DC to be placed in a 28-pin CCD142DC socket. To do so, the CCD122DC is positioned in the center of the 28-pin socket such that Pin 1 of the device aligns with Pin 2 of the socket and Pin 12 of the device with Pin 13 of the socket.

Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD122DC or CCD142DC. The boards are fully assembled and tested and require only one power supply for operation (+ 15 V). The printed circuit board order codes are: CCD122DB, CCD142DB. For further information on the boards please call your nearest Fairchild sales office. For any technical assistance, call (415) 493-8001.

CCD122DC PACKAGE OUTLINE
24-Pin Dual In-line Ceramic Package



CCD142DC PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES:

All dimensions in inches (bold) and millimeters (parenthesis). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

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CCD

(THE CCD142 DEVELOPMENT BOARD IS NO LONGER AVAILABLE)

CCD122 AND CCD142DB DESIGN DEVELOPMENT BOARDS

The Fairchild CCD122DB and CCD142DB design development boards are printed circuit cards which are intended for use as educational aids for gaining understanding of the operating characteristics of Fairchild CCD122 and CCD142 line scan image sensors and for use in assembly of experimental systems using the line scan sensors. The design development boards are sold fully assembled and tested, and require only connection of a single power supply input of +15V and connection of an oscilloscope to display the video information detected by the sensor.

The boards, Figure 1, are 4 1/2 by 5 inches. A socket for installation of the charge coupled device line scan sensor is mounted centrally on the back (wiring) side of the card. The user can readily mount a lens in front of the sensor if required for his study. Board I/O connections are made through a 22 position double readout edge card connector with .156 inch center-to-center finger spacings. The edge connector is compatible with a TRW/CINCH type 50-44B-10 or equivalent.

When a CCD142 is being used with a design development board, it should be installed in the sensor connector in normal fashion. When a CCD122 is being used, it should be inserted into the center of the socket so that socket terminals 1, 14, 15, and 28 are left open.

The board circuit, Figure 2, requires a power supply positive input of 15±2V at 250mA maximum to Pins 1 and A of the edge card connector. The negative power supply line should be wired to the principle board ground contact on Fingers 22 and Z.

Three regulators on the design development boards provide V_{DD} sensor supply voltage which is adjusted to +12.0V, a clock high level voltage which is set to +10.0V, and a +5V V_{CC} required by the TTL logic circuitry.

For normal self-contained operation of the board, Connector Terminals 3 and 5 are left open. Voltage Controlled Oscillator U1 generates a video clock signal which may be adjusted to provide data rates of approximately .5 to to 2.0 MHz by potentiometer R1. VCO U1 operates at twice the video data rate and four times the ϕ_T transport clock frequency. The frequency of the videc clock square wave from U1 is divided by four by flip-flop U2A and U2B; one-half of MOS driver U4 amplifies the flip-flop output to provide the ϕ_T transport clock signal required by the CCD image sensor. The normal amplitude of the ϕ_T clock signal at the sensor terminal is from a low of about 0.5V to a high of about 11.5V, in accordance with the sensor data sheet recommendations. The ϕ_R reset clock signal is generated by U1 and flip-flip U2A and is amplified through U5 to deliver a ϕ_R clock frequency twice that of ϕ_T to the sensor.

One-shot U7A and JK flip-flops U3A and U3B develop a properly synchronized ϕ_X signal which is amplified by the second half of the 9644 driver U4. The interval between ϕ_X pulses is the exposure time for the sensor; exposure time may be adjusted by R2.

In keeping with good high frequency engineering practice, damping resistors R5, R6, and R7 are used in the MOS driver output lines to minimize overshoot and ringing contents in the clock signals supplied to the CCD. Clamp diodes CR4, CR5 and CR6 are used to prevent CCD clock signal excursions below ground; negative clock line transients at the CCD terminals can cause charge-injection which may result in an apparent increase in the dark signal non-uniformity of the sensor.

If U1 is removed from the circuit, the ϕ_T driver will respond to an external data rate clock input on Pin 5. The video data rate for the sensor will be one-half the frequency of the clock signal supplied to Pin 5. If U7 is removed, an external exposure control may be inputed to Pin 3. Sensor exposure intervals are terminated by low-to-high transition on Pin 3.

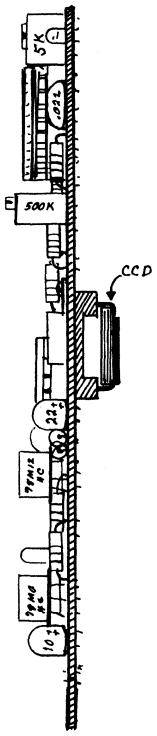
Connector Figure 7 and 9 provide exposure time and data rate clock output signals for external usage; i.e., for synchronizing an oscilloscope for display of the sensor output signals.

The dc bias voltages applied to the V_T transport register electrodes and VEI bias voltage electrodes are preset to give optimal performance of the transport clock, white reference and end-of-scan signals. VEI may be increased to V_{DD} to disable the white reference level generating circuitry within the sensor.

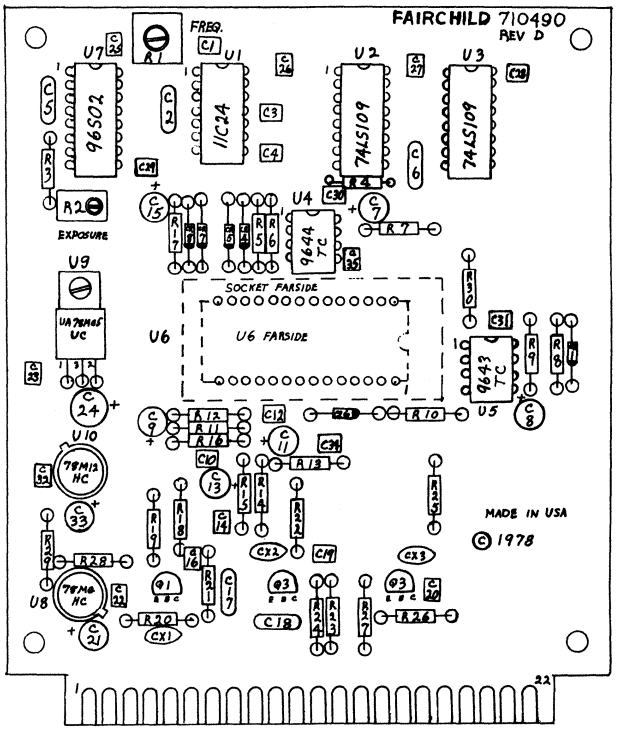
The video output register signal (V_{OUT}) passes through a simple 2MHZ cutoff low pass filter formed by Q1, Q2 and associated capacitance and resistance circuits and is then routed off the board at connector finger 11 through 75 ohm resistor R24. Capacitors CX1, CX2 and CX3 may be installed by the user to provide high frequency rolloff as required to reduce high frequency on the output video signal.

The end-of-scan pulse (V_{EOS}) is buffered by Q3 and sent off the board at connector finger 13 through 75 ohm resistor R27. This pulse indicates that the readout of a line of video information is completed. The EOS pulse was injected into the EOS register by transfer pulse ϕ_X applied to the sensor U6 at pin 16.

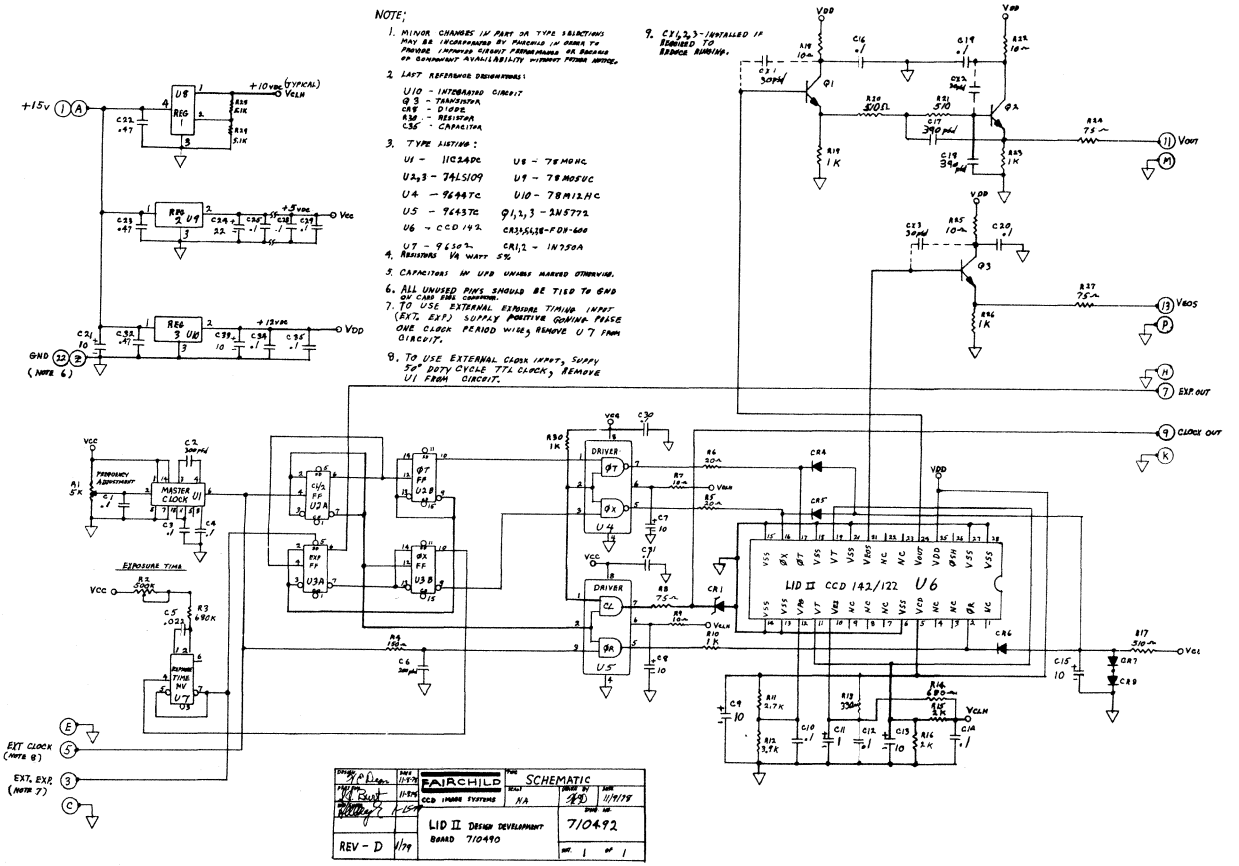
SIDE VIEW



FRONT VIEW



DESIGN	11-8-78	FAIRCHILD	ASSEMBLY DRAWING		
PRODUCTION	11-9-78	CCD IMAGE SYSTEMS	SCALE 1:1	DRAWN BY	DATE 1-15-79
ENGINEERING	1-18-79				DWG. NO.
		LID II DESIGN DEVELOPMENT BOARD		710490	
REV D	1-79			SHT. 1 OF 1	


NOTE:
1. MINOR CHANGES IN PART OR TYPE SELECTIONS MAY BE INCORPORATED BY FAIRCHILD IN ORDER TO PROVIDE IMPROVED CIRCUIT PERFORMANCE OR ENHANCE ITS GOVERNMENT AVAILABILITY WITHOUT FURTHER NOTICE.
2. LAST REFERENCE DESIGNATIONS:
U10 - INTEGRATED CIRCUIT
Q3 - TRANSISTOR
CR6 - DIODE
R32 - RESISTOR
C36 - CAPACITOR
3. TYPE LISTING:
U1 - 1IC24DC
U2,3 - 74LS109
U4 - 9644TC
U5 - 9643TC
U6 - CCD 142
U7 - 96L02
U8 - 78M06C
U9 - 78M05UC
U10 - 78M12HC
Q1,2,3 - 2N5772
CR3,5,6,8-FDH-666
CR1,2 - 1N750A
4. RESISTORS ¼ WATT 5%
5. CAPACITORS IN UFD UNLESS MARKED OTHERWISE.
6. ALL UNUSED PINS SHOULD BE TIED TO GND OR CARD BIAS CONDITIONS.
7. TO USE EXTERNAL EXPOSURE TIMING INPUT (EXT. EXP) SUPPLY POSITIVE GOING PULSE ONE CLOCK PERIOD WIDER REMOVE U7 FROM CIRCUIT.
8. TO USE EXTERNAL CLOCK INPUT, SUPPLY 50% DUTY CYCLE TTL CLOCK, REMOVE U1 FROM CIRCUIT.
9. CX1,2,3 - INSTALLED IF REQUIRED TO REDUCE RINGING.
+15v
+10VDC (TYPICAL)
VCLH
+5VDC
Vcc
+12VDC
VDD
GND
(NOTE 6)
MASTER CLOCK U1
FREQUENCY ADJUSTMENT
EXPOSURE TIME
EXT CLOCK (NOTE 8)
EXT. EXP. (NOTE 7)
DRIVER
LID II CCD 142/122 U6
VOUT
VBOS
EXP. OUT
CLOCK OUT
VCL
FAIRCHILD
CCD IMAGE SYSTEMS
SCHEMATIC
LID II DESIGN DEVELOPMENT BOARD 710490
7/10492
REV - D
1/79

FAIRCHILD
A Schlumberger Company

CCD

CCD123
1728-Element
Line Scan Image Sensor

Preliminary

CCD Imaging

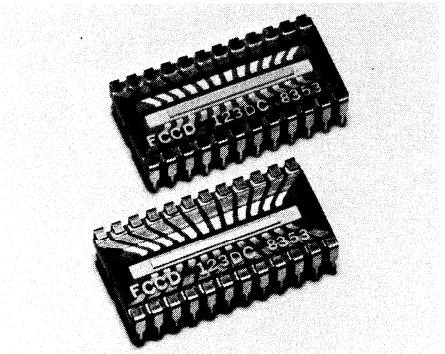
DESCRIPTION

The CCD123 is a monolithic 1728-element line image sensor designed for page scanning applications including facsimile, optical character recognition and other imaging applications which require high resolution and high sensitivity.

The 1728 sensing elements of the CCD123 provide a 200-line per inch resolution across an 8½ inch page adopted as an international facsimile standard.

The CCD123 is similar to the CCD122 but utilizes a smaller photo element and does not incorporate the white reference and end-of-scan functions. The CCD123 can be operated using existing CCD122 circuitry.

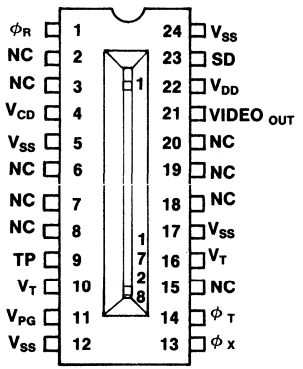
The photo-element size is 10μm (0.39 mils) by 13μm (0.5 mils) on 10μm (0.39 mils) centers. The devices are manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.



FEATURES

- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1V PEAK-TO-PEAK OUTPUTS**
- **DARK REFERENCE CONTAINED IN A SAMPLE-AND-HELD OUTPUT**

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

V_{PG}	Photogate
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
$VIDEO_{out}$	Output Amplifier Source
V_{DD}	Output Amplifier Drain
ϕ_R	Reset Clock
V_{CD}	Clock Driver Drain
V_T	Analog Transport Shift Registers DC Electrode
SD	Sample-and-Hold Clock Disable
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

CCD133/143

See the CCD133A and CCD143A updated technical description for device changes.

1024/2048-ELEMENT HIGH-SPEED LINEAR IMAGE SENSOR

FAIRCHILD CHARGE COUPLED DEVICE

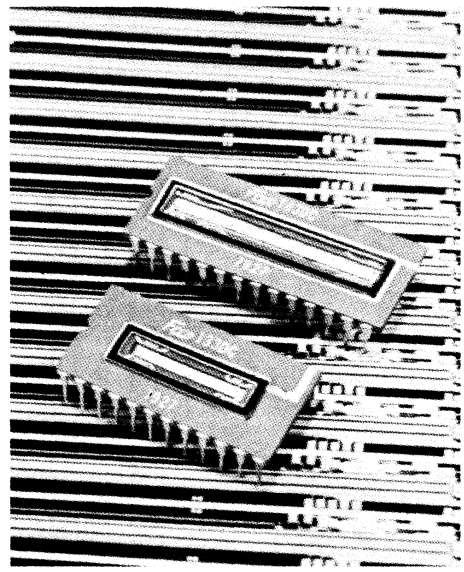
GENERAL DESCRIPTION

The CCD133 and CCD143 are 1024 and 2048-element line image sensors, respectively. The charge-coupled devices are designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolution, high sensitivity, and high data rates.

The 1024 sensing elements of the CCD133 provide a 120-line per inch resolution across an 8 1/2-inch page and the 2048 sensing elements of the CCD143 an 8-line per millimeter resolution across a 256-millimeter page adopted as the Japanese facsimile standard.

The CCD133 and the CCD143 are second generation devices having an overall improved performance compared with the first generation devices including higher sensitivity, an enhanced blue response and a lower dark signal. The devices also incorporate on-chip clock driver circuitry and are capable of high-speed operation up to a 20 MHz data rate. The photoelement size is 13 μm (0.51 mils) by 13 μm (0.51 mils) on 13 μm (0.51 mils) centers. The devices are manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

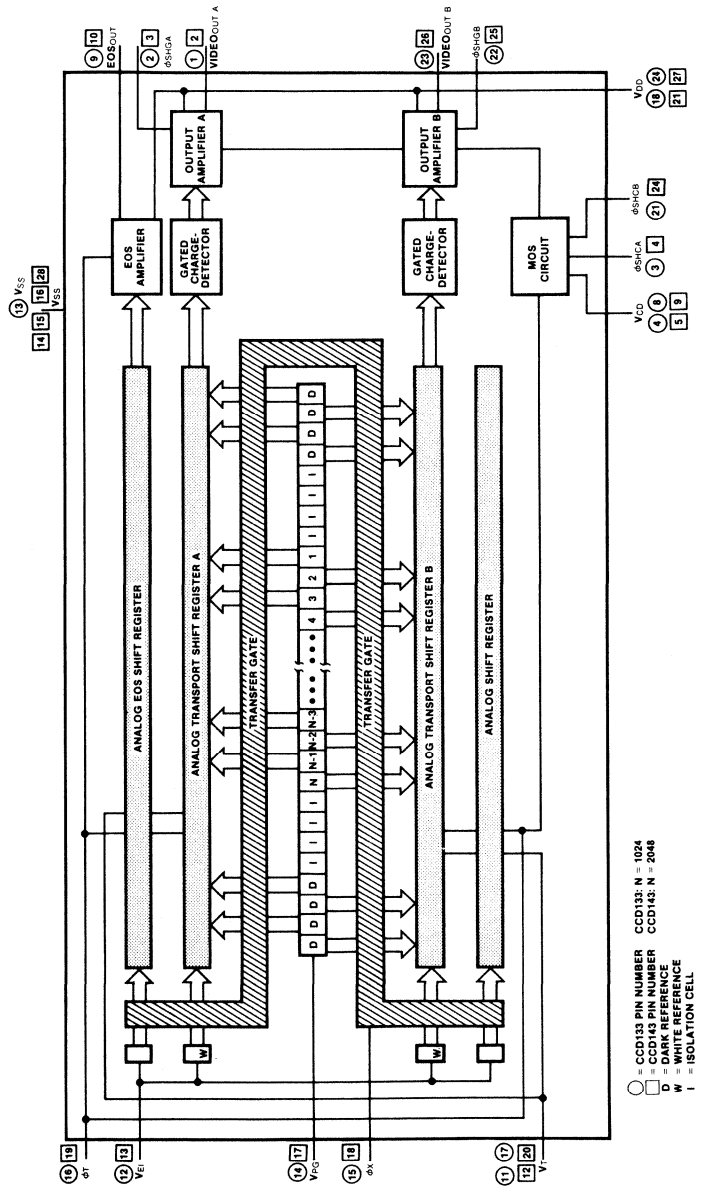
- **HIGH SPEED: UP TO 20 MHz DATA RATE**
- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1 V PEAK-TO-PEAK OUTPUTS**
- **DARK AND WHITE REFERENCES CONTAINED IN SAMPLE-AND-HOLD OUTPUTS**
- **SINGLE POWER SUPPLY**



PIN NAMES

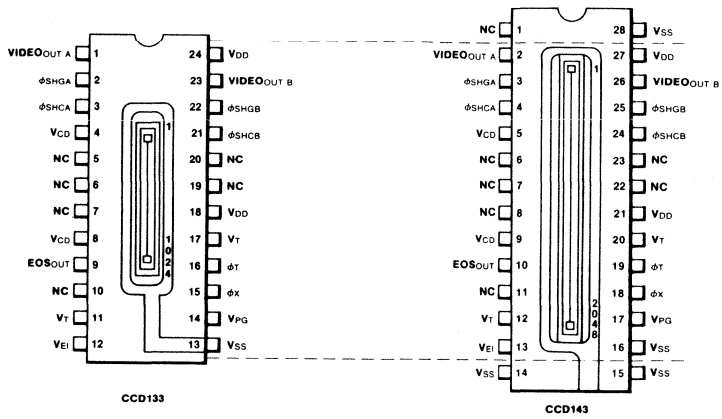
V_{PG}	Photogate
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
$VIDEO_{OUT\ A}$	Output Amplifier A Source
$VIDEO_{OUT\ B}$	Output Amplifier B Source
V_{DD}	Output Amplifier Drain
V_{CD}	Clock Driver Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
EOS_{OUT}	End-of-Scan Output
ϕ_{SHGA}	Sample-and-Hold Gate A
ϕ_{SHCA}	Sample-and-Hold Clock A
ϕ_{SHGB}	Sample-and-Hold Gate B
ϕ_{SHCB}	Sample-and-Hold Clock B
V_{SS}	Substrate (GND)
NC	No Connection (Do not Ground)

FAIRCHILD • CCD133/143



BLOCK DIAGRAM

CONNECTION DIAGRAM DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION

The CCD133/143 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements —These are elements of a line of 1024/2048 image sensors separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gate —This gate is a structure adjacent to the line of image sensor elements. The charge-packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate voltage goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements and permits entry of charge to the End-of-Scan (EOS) shift registers creating the end-of-scan waveform.

Four 529/1041-Bit Analog Shift Registers —Two registers are on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the two charge-detector/amplifiers. The complementary phase relationship of the last elements of the two transport shift registers provides for alternate delivery of charge-packets to the amplifiers so that the original serial sequence of the line of video may be reestablished at the outputs. The outer two registers serve to deliver the end-of-scan waveform and reduce peripheral electron noise in the inner shift registers.

Two Gated Charge-Detector/Amplifiers — From the end of each transport shift register, charge-packets are delivered to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-hold waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Clock Driver Circuitry —This circuitry allows operation of the CCD133/143 using only two external clocks, (1) a square wave Transport Clock which controls the readout rate of video data from the sensor, and (2) a Transfer Clock pulse which controls the integration time of the sensor.

Dark and White Reference Circuitry — Four additional sensing elements at both ends of the 1024/2048 array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the 1024/2048 illuminated sensor elements (labeled "D" in the Block Diagram). Also included at one end of the 1024/2048 sense element array is a white signal reference level generator which likewise provides a reference in the output signal (labeled "W" in the Block Diagram). These reference levels are useful as inputs to external dc restoration and/or automatic gain control circuitry.

FAIRCHILD • CCD133/143

DEFINITION OF TERMS

Charge-Coupled Device—A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock ϕX—The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock ϕT—The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gated charge-detector/amplifiers.

Gated Charge-Detector/Amplifiers—These are the output circuits of the CCD133/143 which receive the charge-packets from the CCD transport shift registers and provide a signal voltage proportional to the size of each charge-packet received. Before each new charge-packet is sensed, an internal reset clock returns the charge-detector voltages to a fixed base level.

Sample-and-Hold Clock ϕSHC—This is an internally supplied voltage waveform applied to the sample-and-hold gate in the amplifiers to create a continuous sampled video signal at the output. The sample-and-hold feature can be defeated by connecting $\phi SHGA$ and $\phi SHGB$ to V_{DD} and leaving pins $\phi SHCA$ and $\phi SHCB$ unconnected.

Dark Reference—Video output level generated from sensing elements covered with opaque metalization provides a reference voltage equivalent to device operation in the dark. This permits use of external dc restoration circuitry.

White Reference—Video output level generated by on-chip circuitry provides a reference voltage permitting external automatic gain control circuitry to be used. The reference voltage is produced by charge-injection under the control of the electrical input bias voltage (V_{EI}). The amplitude of the reference is typically 70% of the saturation output voltage.

Isolation Cell—This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark and white reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range—The dynamic range is the saturation exposure divided by the peak-to-peak noise equivalent exposure. (This does not take into account any dark signal components.) Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

Peak-to-Peak Noise Equivalent Exposure—This is the exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure—Saturation exposure is the minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency—This is the percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range—This is the spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity—Responsivity is the output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

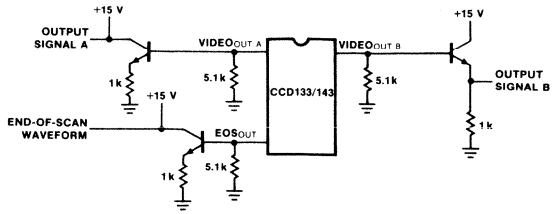
Dark Signal—This is the output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Total Photoresponse Non-Uniformity—This is the difference in the responsive levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

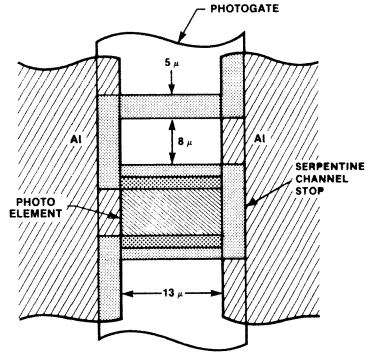
Integration Time—The time interval between the falling edges of any two successive transfer pulses ϕX is the integration time shown in the Timing Diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel—This is a picture element (photosite).

TEST LOAD CONFIGURATION



PHOTOELEMENT DIMENSIONS



All dimensions are typical values.

FAIRCHILD • CCD133/143

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	-25°C to +125°C
Operating Temperature (See curves)	-25°C to +70°C
CCD133: Pins 2, 3, 4, 8, 11, 12, 14, 15, 16, 17, 18, 21, 22, 24	-0.3 V to 18 V
Pin 13	0 V
Pins 1, 5, 6, 7, 9, 10, 19, 20, 23	NC
CCD143: Pins 3, 4, 5, 9, 12, 13, 17, 18, 19, 20, 21, 24, 25, 27	-0.3 V to 18 V
Pins 14, 15, 16, 28	0 V
Pins 1, 2, 6, 7, 8, 10, 11, 22, 23, 26	NC

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ A&B and EOS_{OUT} to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: T_P = 25°C (Notes 1, 2)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{CD}	Clock Driver Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Clock Driver Drain Supply Current		7.0	15	mA	
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14	14.5	V	Note 3
I_{CD}	Output Amplifier Drain Supply Current		15	25	mA	
V_{PG}	Photogate Bias Voltage	8.5	9.0	9.5	V	
V_T	DC Electrode Bias Voltage	5.5	6.0	6.5	V	Note 4
V_{EI}	Electrical Input Bias Voltage		10.5		V	Note 5
V_{SS}	Substrate (Ground)		0.0		V	

CLOCK CHARACTERISTICS: T_P = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi XL}$, $V_{\phi TL}$	Transfer & Transport Clock LOW	0.0	0.3	0.5	V	Notes 6, 7
$V_{\phi XH}$, $V_{\phi TH}$	Transfer & Transport Clock HIGH	11	11.5	12	V	Note 7
$f_{DATA\ MAX}$	Maximum Output Data Rate	12	20		MHz	Notes 8, 9

NOTES

1. T_P is defined as the package temperature.
2. All V_{SS} pins must be grounded. All V_{DD} pins must be connected and tied to V_{CD}. All NC pins must be left unconnected.
3. $V_{DD} = V_{CD}$.
4. $V_T = 0.55\ V_{\phi XH} = 0.55\ V_{\phi TH}$.
5. V_{EI} is used to generate the end-of-scan output and the white reference output. These two signals can be eliminated by connecting V_{EI} to a voltage level equal to $V_{\phi XH}$ + 5 V.
6. Negative transients on any clock pin going below 0.0 V may cause charge-injection which results in an increase in apparent DS.
7. $C_{\phi T}$ = 350 pF for CCD133, $C_{\phi T}$ = 700 pF for CCD143, $C_{\phi X}$ = 150 pF for CCD133, $C_{\phi X}$ = 300 pF for CCD143.
8. Minimum clock frequency is limited by increase in dark signal.
9. $f_{DATA} = 2 \times f_{\phi T}$.
10. Dynamic range is defined as V_{SAT}/peak-to-peak temporal noise or V_{SAT}/rms temporal noise.
11. 1 $\mu j/cm^2$ = 0.02 fcs at 2854°K, 1 fcs = 50 $\mu j/cm^2$ at 2854°K.
12. SE for 2854°K broadband light without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 0.8 $\mu j/cm^2$.
13. CTE is the measurement for a one-stage transfer.
14. See photographs for PRNU definitions.
15. Video mismatch is the difference in ac amplitudes between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
16. DC mismatch is the difference in dc output level V_O between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$.
17. See photographs for DS definitions.
18. Dark signal component approximately doubles for every 5°C increase in T_P.
19. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in T_P.
20. Responsivity for 2854°K broadband light source without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 2 V per $\mu j/cm^2$.
21. See test load configurations.

AC CHARACTERISTICS: (Note 1)
T_P = 25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854°K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)	500:1 2500:1	1000:1 5000:1			Note 10
NEE	RMS Noise Equivalent Exposure		0.00013		$\mu j/cm^2$	Note 11
SE	Saturation Exposure		0.67		$\mu j/cm^2$	Note 12
CTE	Charge Transfer Efficiency		0.99999			Note 13
V_O	Output DC Level	4.0	8.0	11.0	V	
Z	Output Impedance		0.75	1.5	kΩ	
P	On-Chip Power Dissipation Clock Drivers Amplifiers		 100 170	 215 325	 mW mW	
N	Peak-to-Peak Temporal Noise		2.0		mV	

PERFORMANCE CHARACTERISTICS: (Note 1)
T_P = 25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854°K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU**	Photoresponse Non-Uniformity:					Note 14
	Peak-to-Peak		180	240	mV	
	Peak-to-Peak Without Single-Pixel Positive & Negative Pulses		120		mV	
	Single-Pixel Positive Pulses		100		mV	
	Single-Pixel Negative Pulses		150		mV	
M_{VIDEO}	Video Mismatch		40	160	mV	Note 15
M_{DC}	DC Mismatch		0.5	2.0	V	Note 16
DS	Dark Signal:					Notes 17, 18
	DC Component		2.0	5.0	mV	
	Low Frequency Component		2.0	5.0	mV	
SPDSNU	Single-Pixel DS Non-Uniformity		5.0	20	mV	Notes 17, 19
R	Responsivity	1.8	3.0	4.5	Volts per $\mu j/cm^2$	Note 20
V_{SAT}	Saturation Output Voltage	1.0	2.0	2.5	V	Note 21

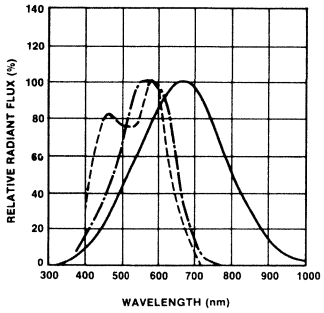
* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror

** PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array. Also excluded from the measurement are video and dc mismatch.
All PRNU measurements are taken at a 800 mV output level using an f/5.0 lens.
The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly columnated light causes the package window aberrations to dominate and increase PRNU. A lower "f" number results in less columnated light causing device photosite blemishes to dominate the PRNU.

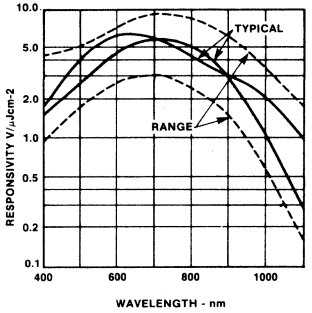
FAIRCHILD • CCD133/143

TYPICAL PERFORMANCE CURVES

***RELATIVE RADIANT FLUX VS WAVELENGTH**

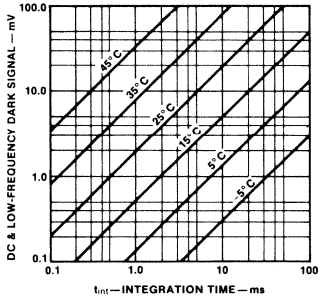


TYPICAL SPECTRAL RESPONSE



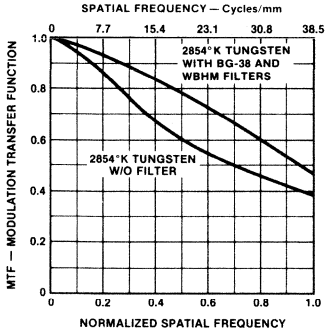
— — — TYPICAL "DAYLIGHT FLUORESCENT" BULB
— — — 2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
——— 2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME

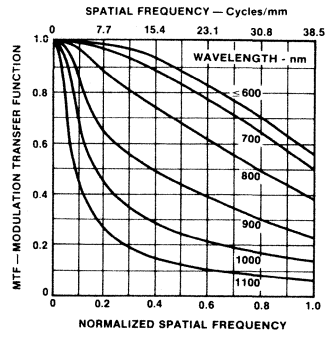


TYPICAL PERFORMANCE CURVES

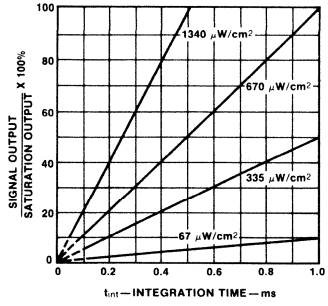
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



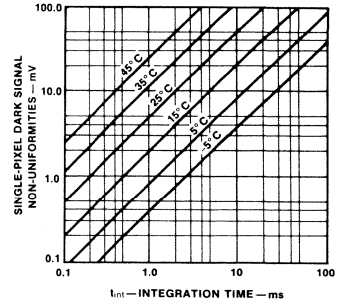
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS

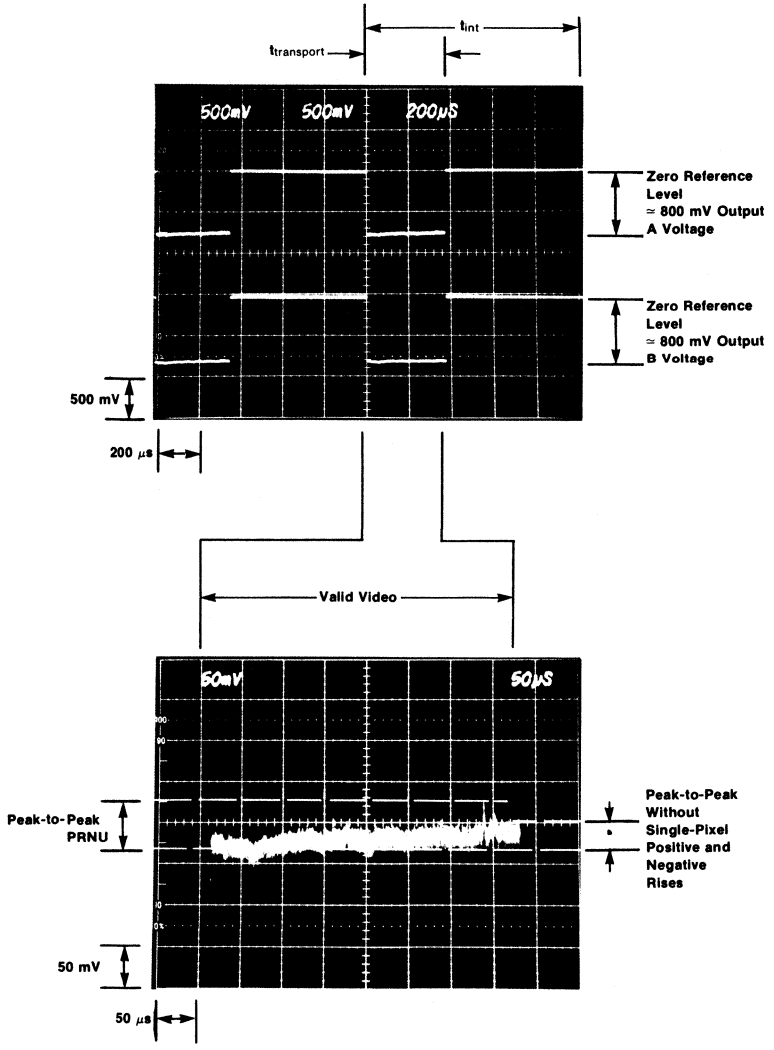


SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



FAIRCHILD • CCD133/143

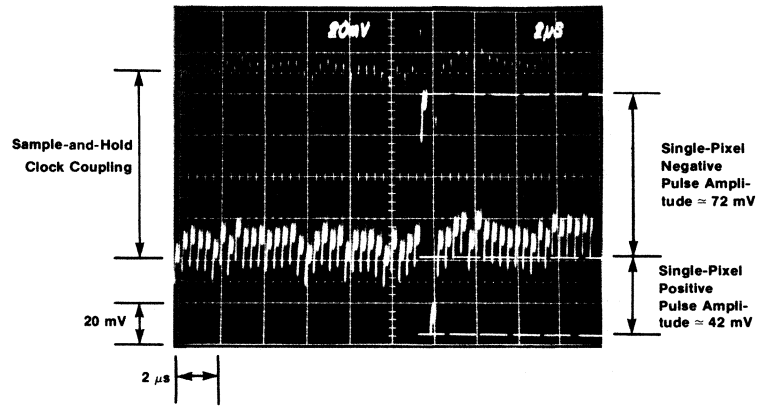
PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS

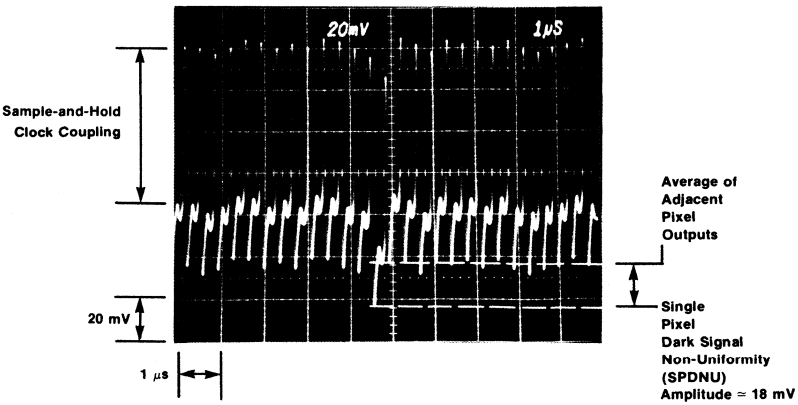
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten + 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

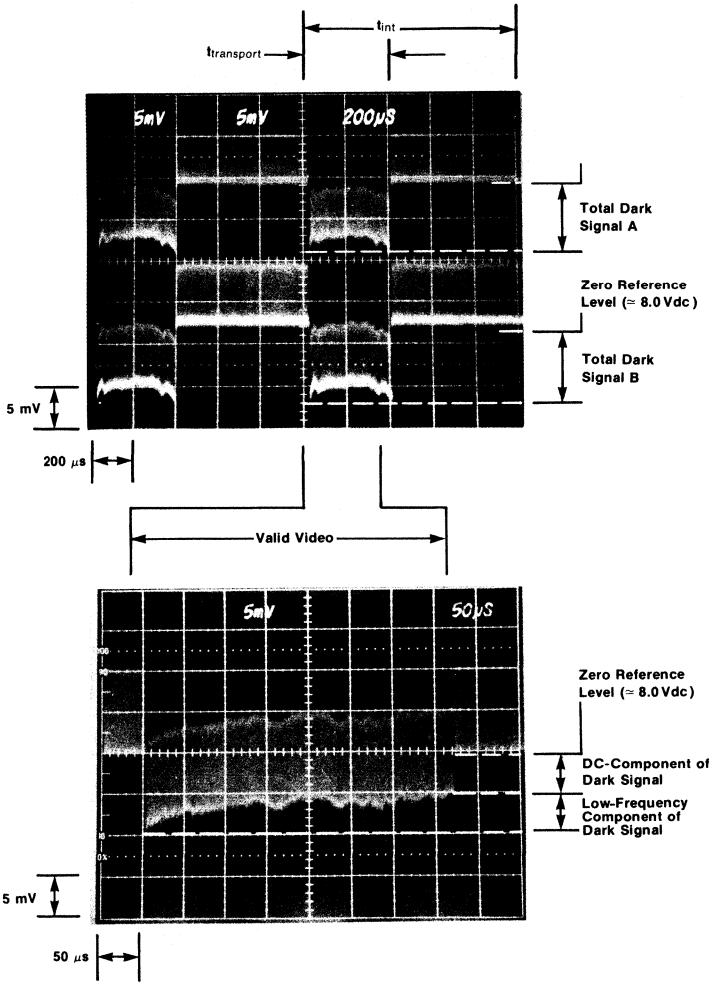
DARK SIGNAL PARAMETERS (DS)



TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter

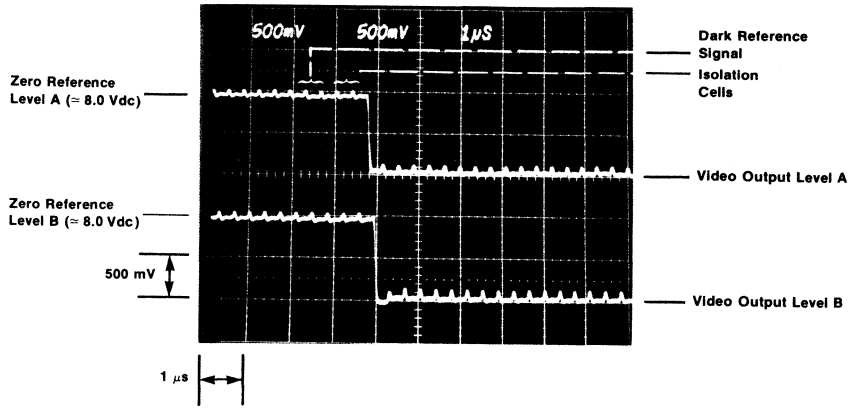
FAIRCHILD • CCD133/143

DARK SIGNAL PARAMETERS (DS)

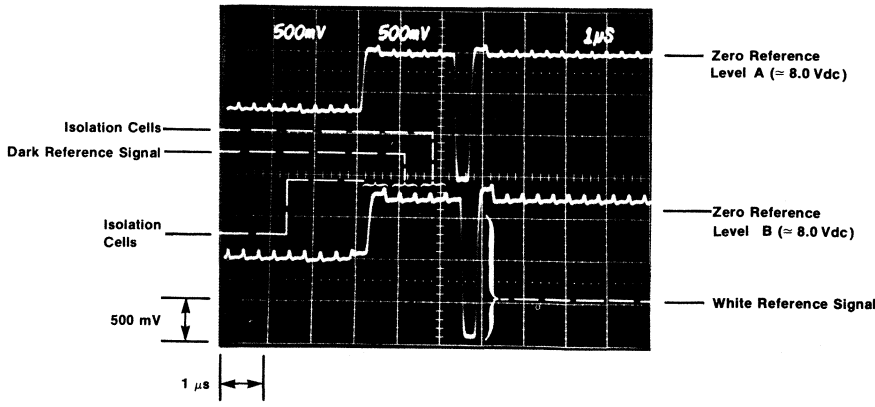


TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

VIDEO OUTPUT TIMING PHOTOGRAPHS



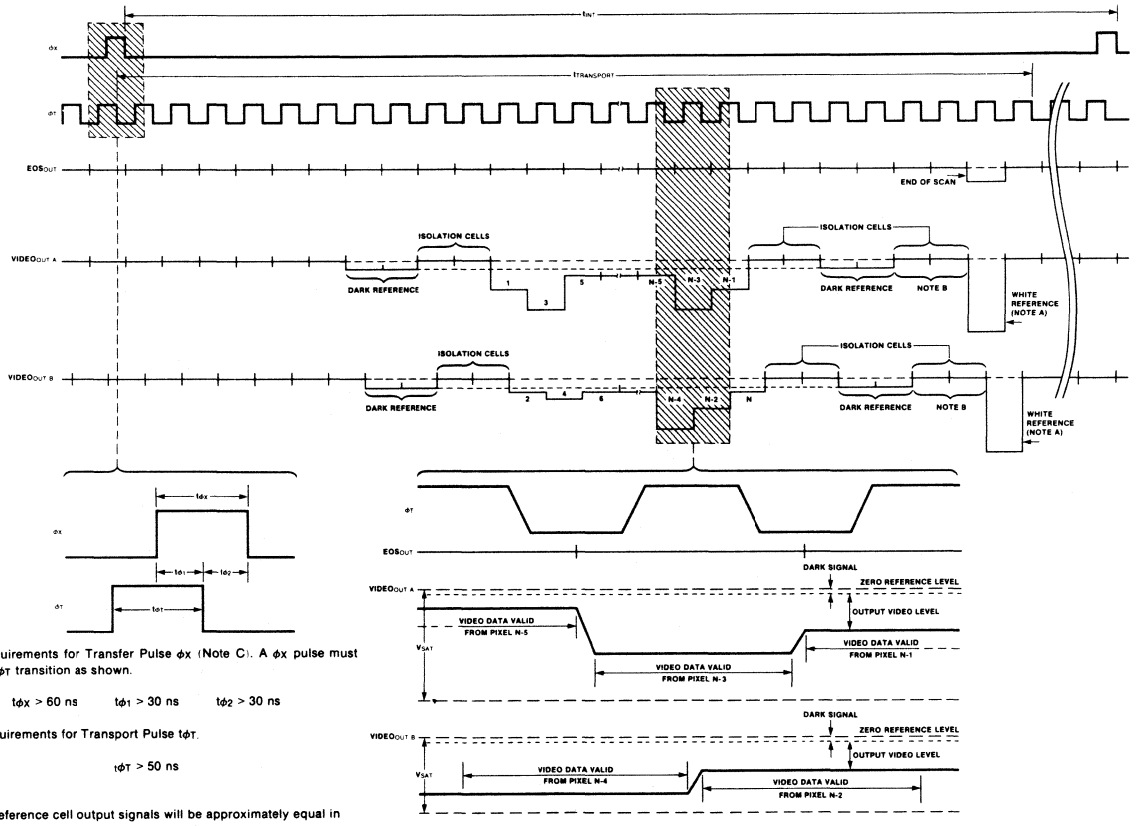
Start of One Scan Video Output



End of One Scan Video Output

TEST CONDITIONS

T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten with 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter



TIMING DIAGRAM

Timing requirements for Transfer Pulse ϕx (Note C). A ϕx pulse must straddle a ϕT transition as shown.

$t\phi x > 60$ ns $\quad t\phi_1 > 30$ ns $\quad t\phi_2 > 30$ ns

Timing requirements for Transport Pulse $t\phi T$.

$t\phi T > 50$ ns

NOTES:

A. White reference cell output signals will be approximately equal in height.

B. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.

C. Recommended rise and fall times for all clocks are that they are ≥ 20 ns.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD133DC, or CCD143DC, where "D" stands for a ceramic package and "C" for commercial temperature range. The pins on the CCD133DC and the CCD143DC are arranged to allow the 24-pin CCD133DC to be placed in a 28-pin CCD143DC socket. To do so, CCD133DC is positioned in the center of the 28-pin socket such that Pin 1 of the device aligns with Pin 2 of the socket and Pin 12 of the device with Pin 13 of the socket.

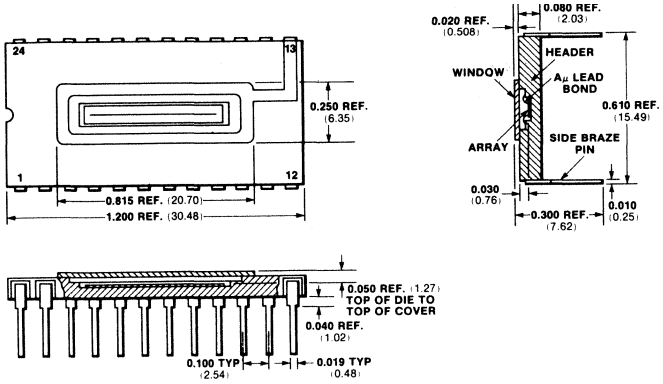
Also available are printed circuit boards that include all the necessary clocks, logic drivers and video amplifiers to operate the CCD133DC or CCD143DC. The boards are fully assembled and tested and require only one power supply for operation (+20 V). The printed circuit board order codes are: CCD133DB, CCD143DB.

For further information on the boards, please call your nearest Fairchild Sales Office. For any technical assistance, call (415) 493-8001.

FAIRCHILD • CCD133/143

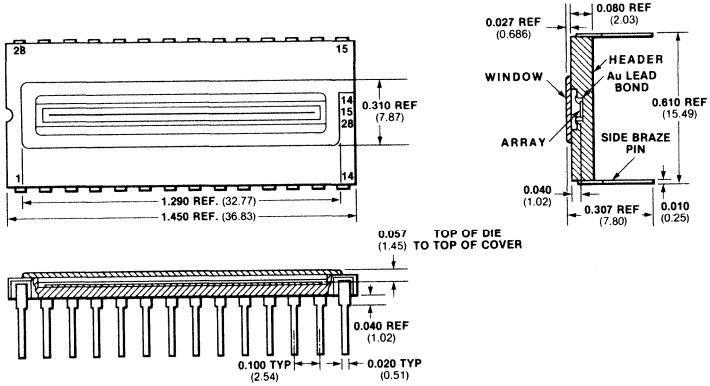
CCD133DC PACKAGE OUTLINE

24-Pin Dual In-line Ceramic Package



CCD143DC PACKAGE OUTLINE

28-Pin Dual In-line Ceramic Package



NOTES:
All dimensions in inches (**bold**) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

All CCD133DCs shipped since the Summer of 1983 have been tested to the CCD133A spec described below. However, to simplify ordering procedures we will continue to use the CCD133DC as the appropriate ordering code.

UPDATED TECHNICAL DESCRIPTION OF THE CCD133A

GENERAL DESCRIPTION

The CCD133A is a 1,024-photoelement linear image sensor utilizing charge-coupled device technology. It is designed for visible and very-near-IR imaging applications such as page scanning, facsimile, optical character recognition, earth-resources-satellite telescopes, and other applications which require high resolution, high responsivity, high data rates, and high dynamic range.

The CCD133A has been improved and is pin-for-pin compatible with the CCD133 except for the deletion of the end-of-Scan Waveform (EOS_{OUT}). The CCD133A has several new features-which may be implemented at the user's option by supplying input voltages and waveforms different than those required for standard CCD133-type operation.

Photoelemnt size is 13μmx 13μm on 13μm centers. The devices are manufactrued using Fairchild advanced second-generation charge-coupled-device n-channel Isoplanar silicon-gate buried-channel technology.

CCD133A OPTIONAL PERFORMANCE FEATURES

1. IMPROVED LINEARITY

   Optimal amplifier linearity is achieved when the Gated Charge Integrator is reset to a lower voltage than V_{DD}. The CCD133A Reset Drain (V_{RD}) is supplied externally from pin 18, which was a V_{DD} pin on the CCD133. Since $I_{RD} << 1\mu A$, V_{RD} is easily generated from a resistor divider from V_{DD} to V_{SS}.

2. LOWER VOLTAGE REQUIRED TO DISABLE WHITE REFERENCE SIGNAL

   Connecting V_{EI} to V_{DD} will disable (eliminate) the white reference signal from the $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ outputs. Formerly V_{EI} was required to be greater than V_{DD} to achieve this. Lower voltage is also required to enable white reference. White reference is now enabled for $4V \leq V_{EI} \leq 8V$; it may now be enabled by tying V_{EI} to the V_T bias supply.

PERFORMANCE CHARACTERISTIC

	MIN	TYP	MAX
R Responsivity	1.8	3.0	5.5 Volts per $\mu j/cm^2$

PIN NAMES AND PIN CONNECTION DIAGRAM

Pin names are given in Table 1-1. Pin connections to the package are given in Figure 1-1.

CCD133A PIN NAMES

$VIDEO_{OUT_A}$	Output Amplifier A Signal Output
$V_{SH_{GA}}$	Sample-and-Hold (input) Gate A
$V_{SH_{CA}}$	Sample-and-Hold (output) Clock A
V_{CD_1}	Clock Driver Drain
V_T	Analog Transport Shift Register DC Electrode Bias
V_{EI_1}	Electrical Input Bias
V_{SS}	Substrate (Ground)
V_{PG}	Photogate
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
V_{RD}	Reset Drain
$V_{SH_{CB}}$	Sample-and-Hold (output) Clock B
$V_{SH_{GB}}$	Sample-and-Hold (input) Gate B
$VIDEO_{OUT_B}$	Output Amplifier B Signal Output
V_{DD}	Output Amplifier Drain
NC	Not Connected (May be grounded)

Table 1-1

CCD133A PIN CONNECTION DIAGRAM

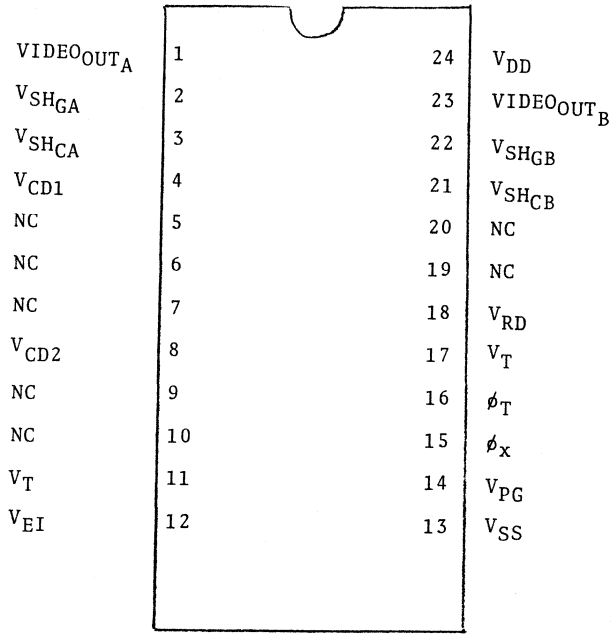
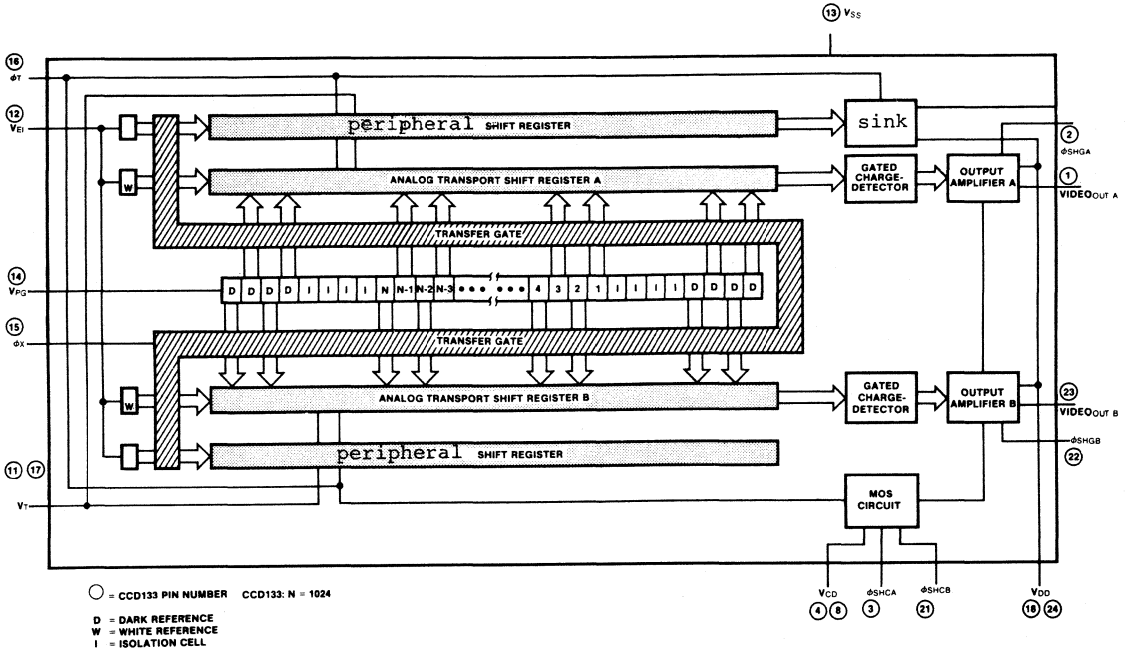


Figure 1-1



BLOCK DIAGRAM

FIGURE 1-2

FUNCTIONAL DESCRIPTION

Refer to the Block Diagram in Figure 1-2. The CCD133A consists of the following key functional elements:

Image Sensor Elements: The 1,024 photosites in the 1x1,024 array ("pixels") are separated by diffused channel stops. The channel stop is photoactive; the edge of each pixel is at the center of the channel stop. Image photons pass through the silicon dioxide surface passivation layer over the pixel and are absorbed in the single crystal silicon, generating hole-electron pairs. These electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is directly proportional to the incident radiant energy and the integration time.

Photogate: The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate: The transfer gate structure separates the outer edge of the photogates from the analog shift registers. Charge-packets generated and accumulated in the photosites are transferred into the transport analog shift registers whenever the transfer gate voltage goes "High." All odd-numbered charge packets are transferred into the "A" transport analog shift register; all even-numbered charge packets are transferred into the "B" transport analog shift register. The transfer gate also controls the input of charge from V_{EI} into the white reference cells (described below). The time interval between successive transfer pulses determines the integration time.

Four 529 Bit Analog Shift Registers: Two registers are on each side of the line of image sensor elements and separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge-packets delivered by the transfer gate serially to the two charge-detector/amplifiers. The complementary phase relationship of the lost elements of the two transport shift registers provides for alternate delivery of charge-packets to the amplifiers so that the original serial sequence of the line of video may be reestablished at the outputs. The outer two registers, the peripheral registers, accumulate charge generated at the chip periphering (by photons passing through unavoidable gaps in the light shield layer, etc.) and transport it to charge sinks.

Two Gated Charge-Detector/Amplifiers: From the end of each transport shift register, charge-packets are delivered to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing

a signal which passes through the sample-and-hold gate to the output at $VIDEO_{OUT}$. The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-hold waveform. The diode is reset to the reset drain bias voltage (V_{RD}) by the reset gate structure.

Clock Driver Circuitry: This circuitry allows operation of the CCD133A using only two external clocks, (1) a square wave Transport Clock which controls the readout rate of video data from the sensor, and (2) a Transfer Clock pulse which controls the integration time of the sensor.

Dark and White Reference Cells & Circuitry: At each end of the 1,024-photosite array there are four additional sensing elements covered by opaque metallization. These "Dark Reference Cells" provide four charge packets (two on each side) at each end of the serial video output which indicate the typical dark (non-illuminated) signal level. In addition, two "White Reference Cells" (one per side) are input into the serial video outputs after the last pixel (#1024) and the dark reference cells. (Refer to the section on the transfer gate, above). Each white reference cell generates an output signal pulse approximately 70% of the amplitude of a photosite saturation (maximum) signal. These cells may be used as inputs to external DC restoration and/or automatic gain control circuits. White reference amplitude is slightly dependant on exposure, especially at infrared wavelengths.

All CCD143DCs shipped since the Spring of 1982 have been tested to the CCD143A spec described below. However, to simplify ordering procedures we will continue to use the CCD143DC as the appropriate ordering code.

DETAILED TECHNICAL DESCRIPTION of the CCD143A

GENERAL DESCRIPTION

The CCD143A is a 2,048-photoelement linear image sensor utilizing charge-coupled device technology. It is designed for visible and very-near-IR imaging applications such as page scanning, facsimile, optical character recognition, earth-resources-satellite telescopes, and other applications which require high resolution, high responsivity, high data rates, and high dynamic range.

The CCD143A is an improved pin-for-pin compatible direct replacement for the CCD143. The CCD143A has several features - not available on the CCD143 - which may be implemented at the user's option by supplying input voltages and waveforms different than those required for standard CCD143-type operation.

Photoelement size is 13µm x 13µm on 13µm centers. The devices are manufactured using Fairchild advanced second-generation charge-coupled-device n-channel Isoplanar silicon-gate buried-channel technology.

CCD143A OPTIONAL PERFORMANCE FEATURES

The CCD143A has five optional performance features which were not available on the CCD143, as follows:

1. EXTERNAL RESET CLOCKS:

   Dynamic Range and S/N Ratio may be maximized by double-correlated sampling off-chip of the device output. This requires externally-supplied reset clocks for the on-chip amplifiers. Pins 5 and 21, formerly $V_{CD/DD}$, are now ϕR_A and ϕR_B, respectively. If this feature is not desired, both pins should be tied to $V_{CD/DD}$, which enables the internally-generated reset circuits.

2. IMPROVED SAMPLE-&-HOLD DISABLE

   If the internal (on-chip) Sample-&-Hold Clocks are not used, the on-chip Sample-&-Hold clock driver circuits can be depowered, which greatly reduces on-chip power consumption. This results in lower dark signal as well. Pin 16, formerly V_{SS}, is now the ground for the ϕ_{SH} clock drivers. To disable (turn off) these drivers, $V_{CG}\phi_{SH}$ is tied to $V_{DD/CD}$. The on-chip ϕSH clock drivers (and logic) are enabled by

connecting $V_{CG\phi SH}$ to V_{SS}.

3. IMPROVED LINEARITY

Optimal amplifier linearity is achieved when the Gated Charge Integrator is reset to a lower voltage than V_{DD}. The CCD143A Reset Drain (V_{RD}) is supplied externally from pin 27, which was a V_{DD} pin on the CCD143. Since $I_{RD} << 1\mu A$, V_{RD} is easily generated from a resistor divider from V_{DD} to V_{SS}.

4. LOWER VOLTAGE REQURIED TO DISABLE WHITE REFERENCE SIGNAL

Connecting V_{EI} to VDD will disable (eliminate) the white reference signal from the $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ outputs. The CCD143 required that $V_{EI} > V_{DD}$ to achieve this.

5. REDUCED CLOCK COUPLING

An additional V_{SS} pin, pin number 8, is provided on the CCD143A to reduce clock coupling on the output pins. This pin was NC (not connected) on the CCD143. In addition, all NC pins may be grounded during operation of the CCD143A to further reduce pin-to-pin capacitive coupling. On the CCD143, all NC pins had to be unconnected during operation.

NB: The End-of-Scan (EOS_{out}) output was eliminated from the CCD143A.

PIN NAMES AND PIN CONNECTION DIAGRAM

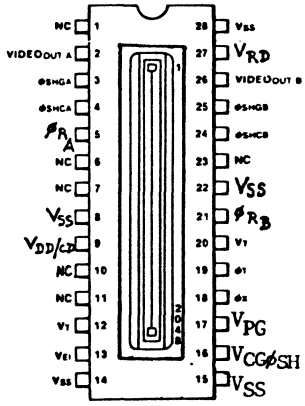
Pin names are given in Table 2-1. Pin connections to the package are given in Figure 2-1.

TABLE 2-1

CCD143A PIN NAMES

$V_{DD/CD}$	Output Amplifer & Clock Drivers Drain
V_{EI}	Electrical Input Bias
V_{RD}	Reset Drain
V_{PG}	Photogate
V_T	Analog Transport Shift Register DC Electrode Bias
ϕ_T	Transport Clock
ϕ_X	Transfer Clock
ϕ_{R_A}	Reset Clock A
ϕ_{R_B}	Reset Clock B
ϕ_{SHC_A}	Sample-&-Hold (output) Clock A
ϕ_{SHC_B}	Sample-&-Hold (output) Clock B
$V_{CG\phi SH}$	Sample-&-Hold (output) Clock Drivers Source/Ground.
ϕ_{SHG_A}	Sample-&-Hold (input) Gate A
ϕ_{SHG_B}	Sample-&-Hold (input) Gate B
V_{SS}	Substrate (Ground)
NC	Not Connected (May be grounded)
$VIDEO_{OUT_A}$	Output Amplifier A Signal Output
$VIDEO_{OUT_B}$	Output Amplifier B Signal Output

FIGURE 2-1 CCD143A PIN CONNECTION DIAGRAM



[Top View; Not to Scale]

FUNCTIONAL DESCRIPTION

Refer to the Block Diagram in Figure 2-2. The CCD143A consists of the following key functional elements:

Image Sensor Elements: The 2,048 photosites in the 1x2,048 array ("pixels") are separated by diffused channel stops, as shown in Figure 2-3. The channel stop is photoactive; the edge of each pixel is at the center of the channel stop. Image photons pass through the silicon dioxide surface passivation layer over the pixel and are absorbed in the single crystal silicon, generating hole-electron pairs. These electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is directly proportional to the incident radiant energy and the integration time.

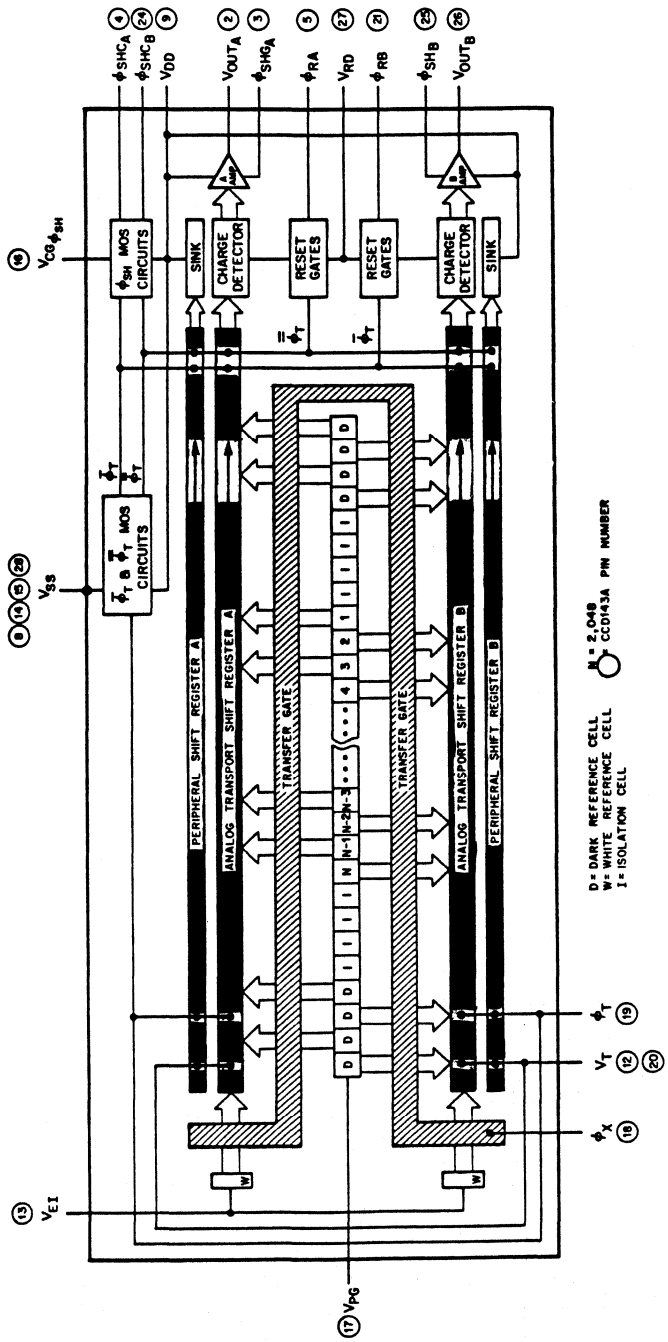
Photogate: The photogate structure, located at the edge of the photosites, provides a bias voltage for the photosites.

Transfer Gate: The transfer gate structure separates the outer edge of the photogates from the analog shift registers. Charge-packets generated and accumulated in the photosites are tranferred into the transport analog shift registers whenever the transfer gate voltage goes "High". All odd-numbered charge packets are transferred into the "A" transport analog shift register; all even-numbered charge packets are transferred into the "B" transport analog shift register. The transfer gate also controls the input of charge from V_{EI} into the white reference cells (described below). The time interval between successive transfer pulses determines the integration time.

Analog Shift Registers: Four 1,041-element analog shift registers transport charge towards the output end of the chip. The two inner registers, the transport registers, move the image-generated charge packets serially to the two gated charge detectors and amplifiers. The two outer shift registers, the peripheral registers, accumulate charge generated at the chip periphery (by photons passing through unavoidable gaps in the light shield layer, etc.) and transport it to charge sinks. The primary shift register clock is ϕ_T. The complementary phase relationship of the secondary shift register clocks $\phi_{\overline{T}}$ and $\phi_{\overline{\overline{T}}}$, generated on-chip, provide alternate delivery of charge packets from "A" and "B" shift registers to their amplifiers so that the original serial sequential string of video information may be easily demultiplexed off-chip.

Gated Charge Detectors & Reset Gates: Each transport analog shift register delivers charge packets to a precharged diode. The change

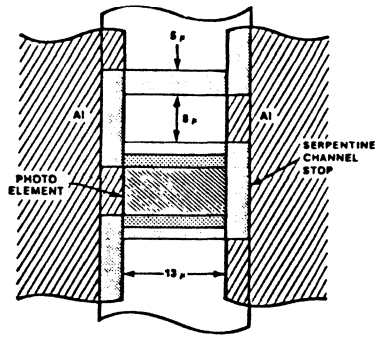
Figure 2-2



CCD143A BLOCK DIAGRAM

Figure 2-2

FIGURE 2-3 PHOTOSITE CONFIGURATION



(Not to Scale; All Dimensions are Typical Values)

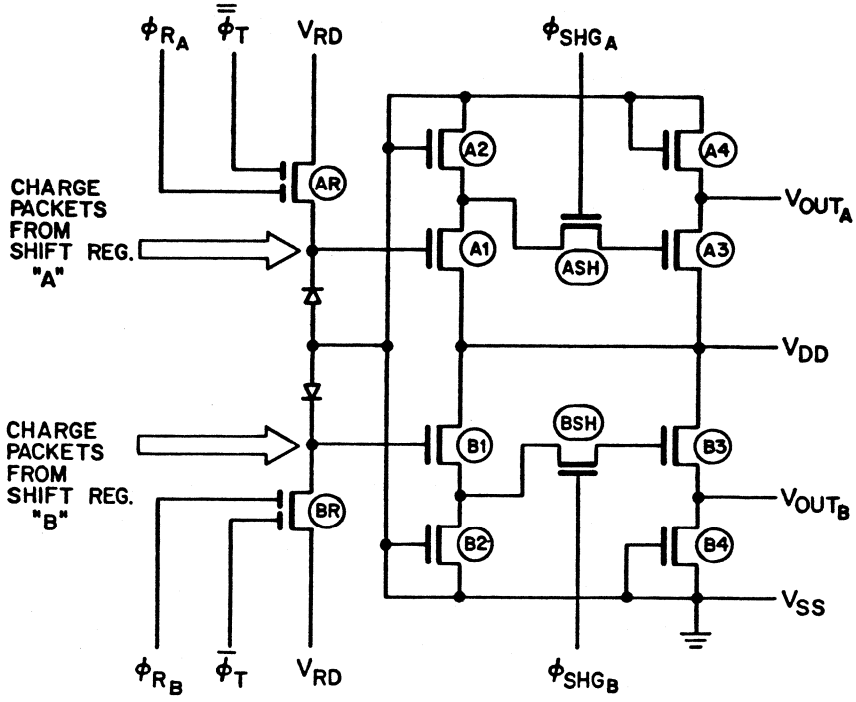
in diode potential is linearly proportional to the amount of charge delivered in the charge packet. This potential is applied to the input gate of a MOS transistor amplifier (see below), which linearly amplifies the input potential. The diode is reset to the reset drain bias voltage (V_{RD}) by the reset gate structure. Reset occurs whenever both the internal reset clocks ($\overline{\phi_T}$ on the "A" side, $\overline{\phi_T}$ on the "B" side) and the external reset clocks (ϕR_A, ϕR_B) are both "High" simultaneously on the same side. Each side is reset before the next charge packet is delivered from its respective transport analog shift register.

Output Amplifiers & Sample-&-Hold Gates: Each sides' gated charge integrator drives the input of a two-stage linear MOS-transistor amplifier. A schematic diagram of this circuit is shown in Figure 4 below. The two stages of each amplifier are separated by sample-&-hold gates. The output of the first stage is connected to the input of the second stage whenever the sample-&-hold gate is "High". The output of the second stages are connected to the $VIDEO_{out}$ pins. The sample-&-hold gates are switching MOS transistors: clocking these gates results in a sampled-&-held output, thus eliminating the reset clock feedthrough.

Clock Driver Circuits: Two MOS transistor clock-driver circuits on-chip allow sample-&-held operation of the CCD143A with only two externally-supplied clocks: the square-wave primary shift register transport clock ϕ_T, which determines the output data rate, and the transfer clock ϕ_X, which determines the integration time. If the internally-generated sample-&-hold clocks are not used, the sample-&-hold clock drivers and logic circuits can be depowered independantly of the other clock driver circuits and logic by connecting $V_{CG\phi SH}$ to $V_{DD/CD}$. This reduces on-chip power dissipation, which reduces the temperature-sensitive dark signal (see below).

Dark and White Reference Cells & Circuitry: At each end of the 2,048-photosite array there are four additional sensing elements covered by opaque metallization. These "Dark Reference Cells" provide four charge packets (two on each side) at each end of the serial video output which indicate the typical dark (non-illuminated) signal level. In addition, two "White Reference Cells" (one per side) are input into the serial video outputs after the last pixel (#2048) and the dark reference cells. (Refer to the section on the transfer gate, above). Each white reference cell generates an output signal pulse approximately 70% of the amplitude of a photosite saturation (maximum) signal. These cells may be used as inputs to external DC restoration and/or automatic gain control circuits. White reference amplitude is slightly dependant on exposure, especially at infrared wavelengths.

Figure 2-4



NB: CIRCLED LABELS ARE TRANSISTOR IDENTIFICATION NAMES.

CCD143A OUTPUT AMPLIFIER SCHEMATIC

CCD133DB AND CCD143DB DESIGN DEVELOPMENT BOARDS

The Fairchild CCD133DB and CCD143DB design development boards are printed circuit cards which are intended for use as educational aids for gaining understanding of the operating characteristics of Fairchild CCD133 and CCD143 line scan image sensors and for use in assembly of experimental systems using the line scan sensors. The design development boards are sold fully assembled and tested, and require only connection of a single power supply input of +20V and connection of an oscilloscope to display the video information detected by the sensor.

The boards, Figure 1, are 4 1/2 by 5 inches. A socket for installation of the charge coupled device line scan sensor is mounted centrally on the back (wiring) side of the card. The user can readily mount a lens in front of the sensor if required for his study. Board I/O connections are made through a 44 position double readout edge card connector with .156 inch center-to -center finger spacings. The edge connector is compatible with a TRW/CINCH type 50-44B-10 or equivalent.

When a CCD143 is being used with a design development board, it should be installed in the sensor connector in normal fashion. When a CCD133 is being used, it should be inserted into the center of the socket so that socket terminals 1, 14, 15, and 28 are left open.

The board circuit, Figure 2, requires a power supply positive input of 20+2V at 300mA maximum to Pins 1 and A of the edge card connector. The negative power supply line should be wired to the principle board ground contact on edge Fingers 22 and Z.

Three regulators on the design development boards provide a V_{DD} sensor supply voltage which is adjusted to +15.0V, a clock high level voltage which is set to +12.0V, and a +5V V_{CC} required by the TTL logic circuitry.

For normal self-contained operation of the board, Connector Terminal 17 is left open. Voltage Controlled Oscillator U1 generates a video clock signal which may be adjusted from approximately 5 to 20 MHz by potentiometer R1. The frequency of the video clock square wave from U1 is divided by two by flip-flop U2A; one-half of MOS driver U4 amplifies the flip-flop output to provide the ϕ_T transport clock signal required by the CCD image sensor. The normal amplitude of the ϕ_T clock signal at the sensor terminal is from a low of about 0.5V to a high of about 11.5V, in accordance with the sensor data sheet recommendations. Sensor characteristics at other clock conditions can be evaluated by adjustment of R28.

One-shot U7A and JK flip-flop U2B develop a properly synchronized ϕ_X signal which is amplified by the second half of the 9644 driver U4. The interval between ϕ_X pulses is the exposure time for the sensor; exposure time may be adjusted by R2.

In keeping with good high frequency engineering practice, damping resistors R6 and R7 are used in the MOS driver output lines to minimize overshoot and ringing contents in the clock signals supplied to the CCD. Clamp diodes CR3 and CR4 are used to prevent CCD clock signal excursions below ground; negative clock line transients at the CCD terminals can cause charge-injection which may result in an apparent increase in the dark signal non-uniformity of the sensor.

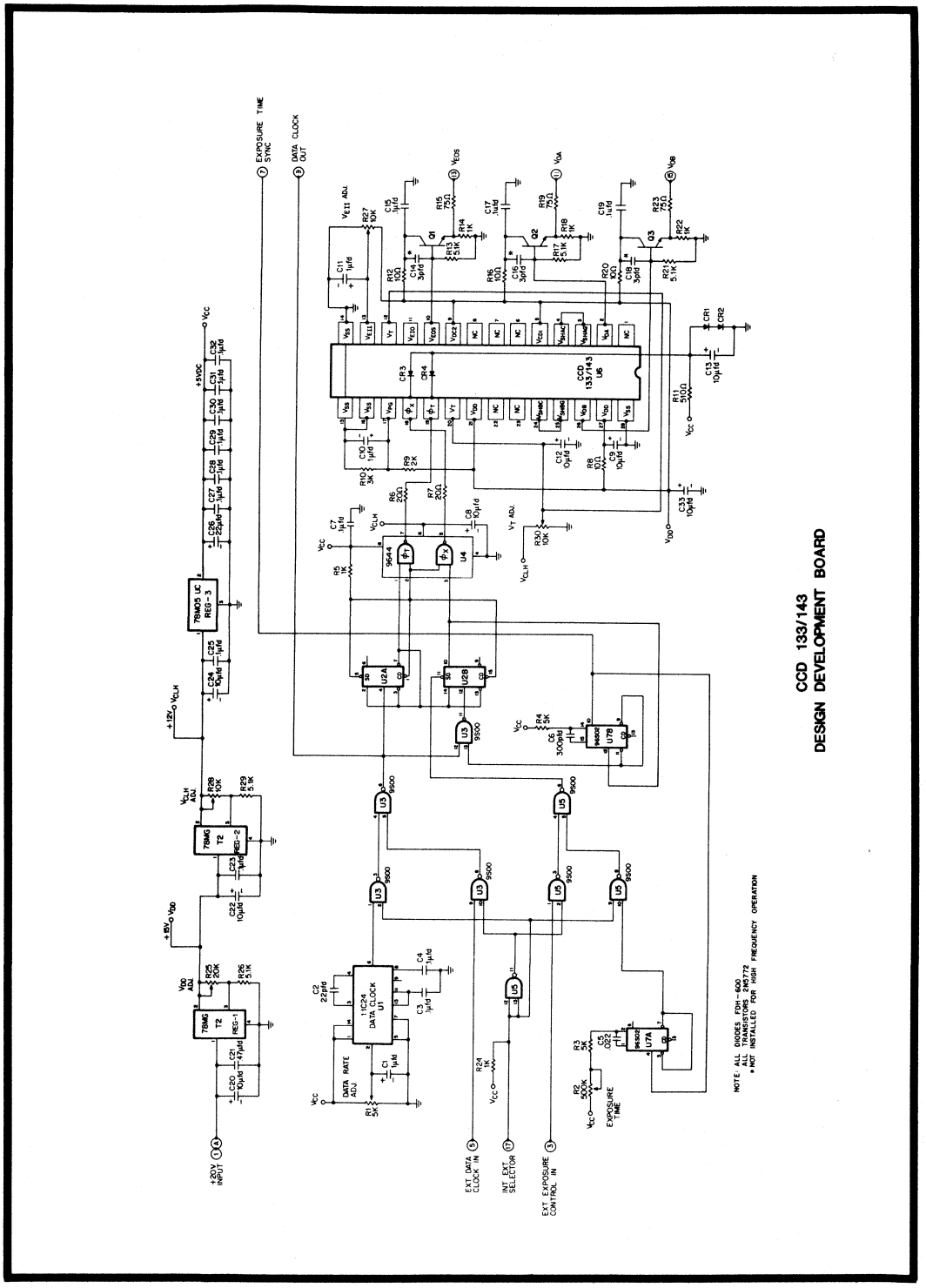
If Finger 17 of the card is held low, the ϕ_T driver will respond to an external data rate clock input on Pin 5 and an external exposure control input to Pin 3. The combined video data rate for the sensor will be equal to the frequency of the clock signal supplied to Pin 5. Sensor exposure intervals are terminated by low-to-high transition on Pin 3.

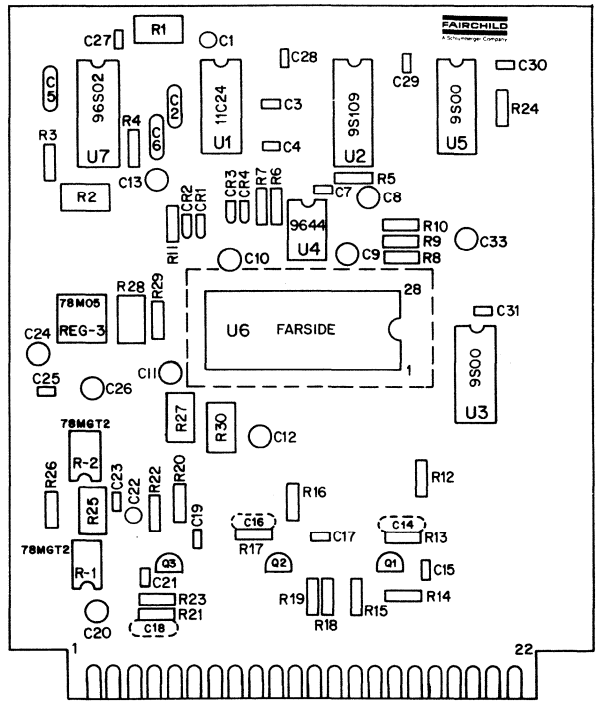
Connector Figures 7 and 9 provide exposure time and data rate clock output signals for external usage; i.e., for synchronizing an oscillosope for display of the sensor output signals.

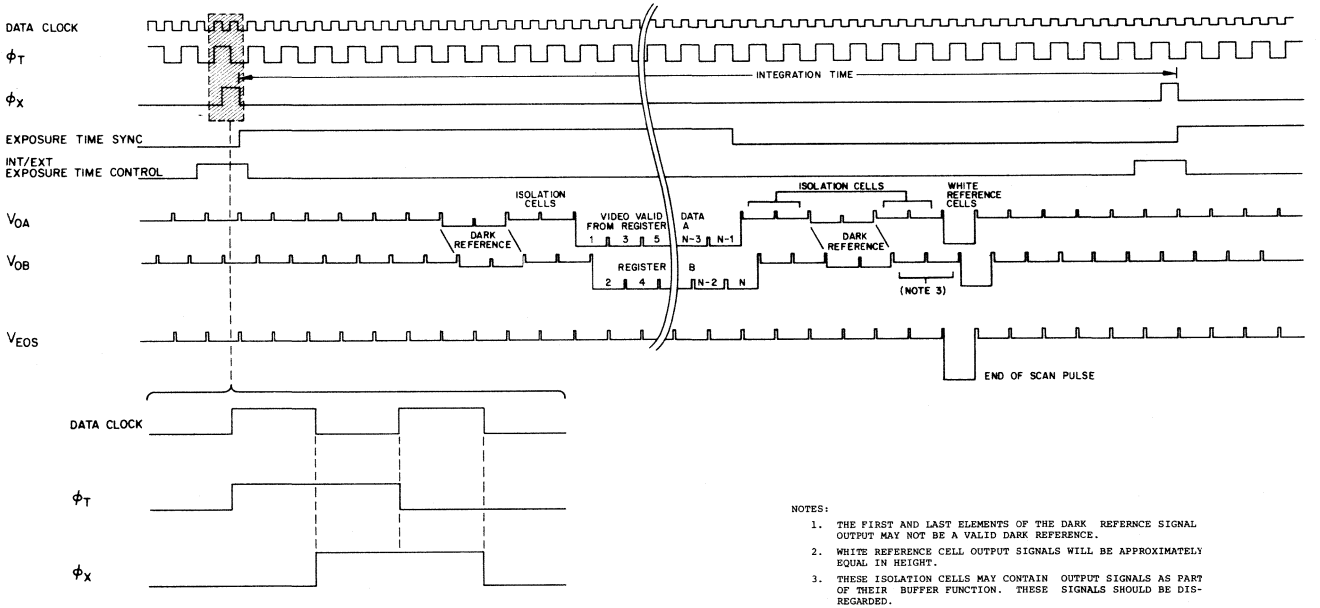
The dc bias voltage applied to the V_T transport register electrodes of the CCD is controlled by R30. This voltage is typically 0.55 times the clock high voltage being supplied to the sensor for best performance. Bias voltage V_{EI} can be set to about 10.5V by R27 to obtain the white reference element output with the video data stream, or it can be increased to V_{DD} to disable the white reference level generating circuitry within the sensor.

The video signals at the two output ports of the CCD line scan sensor are buffered by emitter followers Q2 and Q3 and then made available on connector Fingers 11 and 15. If long co-axial cables are wired to the outputs, the cables should be terminated in 75 ohms for best frequency response. The cable terminations will reduce the video signal amplitude by one-half.

The sensors end-of scan output is also buffered by an emitter follower and is then made available on Pin 13. This signal can be amplified and clipped for use as a system synchronizing pulse if desired.


CCD 133/143
DESIGN DEVELOPMENT BOARD
NOTE: ALL DIODES FDH-600
ALL TRANSISTORS 2N3772
* NOT INSTALLED FOR HIGH FREQUENCY OPERATION
EXPOSURE TIME SYNC
DATA CLOCK OUT
+20V INPUT
EXT. DATA CLOCK IN
INT. EXT. SELECTOR
EXT. EXPOSURE CONTROL IN
EXPOSURE TIME
DATA RATE ADJ.
VDD ADJ.
VCLH ADJ.
VFT ADJ.
VCCD ADJ.
78M05 VOLT REG-3
78M12 VOLT REG-2
78M15 VOLT REG-1
11C24 DATA CLOCK
CCD 133/143


FAIRCHILD
R1
C27
C1
C28
C29
C30
R24
96S02
U7
11C24
U1
9S109
U2
9S00
U5
C3
C4
R4
R3
R2
C13
R5
C7
C8
CR3
CR4
R7
R6
CR2
CR1
R11
9644
U4
R10
R9
R8
C33
C9
C10
R28
R29
78M05
REG-3
C24
C25
C26
C11
U6 FARSIDE
28
1
C31
9S00
U3
R27
R30
C12
78MGT2
R-2
78MGT2
R-1
R26
R25
C23
C22
R22
R20
C19
R16
R12
C16
R17
C17
C14
R13
Q3
C21
Q2
Q1
C15
R23
R21
C20
C18
R19
R18
R15
R14
1
22



TIMING REQUIREMENTS FOR TRANSFER PULSE ϕ_X (NOTE 4)
ϕ_X PULSE MUST STRADDLE ϕ_T PULSE AS SHOWN

NOTES:

1. THE FIRST AND LAST ELEMENTS OF THE DARK REFERNCE SIGNAL OUTPUT MAY NOT BE A VALID DARK REFERENCE.
2. WHITE REFERENCE CELL OUTPUT SIGNALS WILL BE APPROXIMATELY EQUAL IN HEIGHT.
3. THESE ISOLATION CELLS MAY CONTAIN OUTPUT SIGNALS AS PART OF THEIR BUFFER FUNCTION. THESE SIGNALS SHOULD BE DISREGARDED.
4. RECOMMENDED RISE AND FALL TIMES FOR ALL CLOCKS ARE IN THE ORDER OF 10 TO 20 ns.
5. INTEGRATION TIME IS CONTROLLED ON THE BOARD BY SETTING OF R2 EXPOSURE TIME CONTROL, TIME MAY BE CONTROLLED EXTERNALLY BE HOLDING EXTERNAL INPUT IN A LOW STATE FOR THE REQUIRED INTEGRATION TIME.

PRELIMINARY DATA SHEET

THE FAIRCHILD CCD133K COLOR LINE-SCAN IMAGE SENSOR

The Fairchild CCD133K is a modification of the CCD133, a monochrome 1024-element line-scan image sensor. The modification is the addition of a linear array of color filters covering the photoelements and forming the sequence (starting from photoelement #1) green, clear, yellow, cyan, green, etc. The filters are formed on the silicon chip itself and are very thin so that they do not degrade the resolving power of the individual pixels at all. In fact a small region between adjacent photoelements is masked in the color device to improve color separation. As is explained below, this device can provide 512 luminance data samples, and 256 red-green-blue data sample sets.

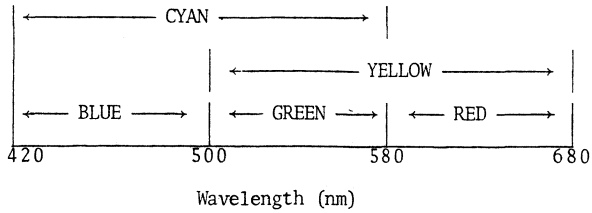
The sequence of colors results in the following readout sequence:

Table I

Output Channel A		Output Channel B	
Pixel #	Color	Pixel #	Color
1	G	2	W
3	Ye	4	Cy
5	G	6	W
7	Ye	8	Cy
etc.		etc.	

where G = green, W = White or clear, Ye = yellow and Cy = cyan. These colors are close approximations to the standard colors in television as defined below:

FIG. 1



The actual typical response spectra with the recommended IR-blocking filter are shown in Fig. 2. The IR-blocking filter is a 2mm-thick Schott BG-38 glass filter. The spectrum of the clear (unfiltered) pixels is seen to peak at approximately 550nm where the eye response peaks and to be quite symmetrical, although it is broader than the eye response (photopic) spectrum. A better approximation to the eye response spectrum is obtained by adding the white and green signals; the resulting spectrum is shown in Fig. 3. Similarily, the sum of the cyan and yellow signals gives virtually the same spectrum. This is called the luminance signal (L). Table II shows how signals from the two output channels of the device are to be sampled and combined so as to generate the derived signals: luminance, blue and red.

Because the cyan, green, and yellow pixels respond outside their ideal response bands, any chrominance signals that are derived from the device output will be somewhat low in amplitude compared to the case of a device with ideal filters and with no optical crosstalk. This lower amplitude can be simply corrected by a modest increase in chrominance amplifier gain anywhere in the system.

PRNU. Whereas the basic CCD133 has a single set of PRNU (photo-response nonuniformity) specifications, associated with one type of pixel and one broadband illumination spectrum, the color device rightfully should have twelve or sixteen sets of specifications, because each type of pixel is possibly subject to different effects for red, green, and blue light, and because a white-light specification might also be desirable. Fortunately, the typical performance suggests that most of this would be quite unnecessary. In fact the largest PRNU is found for blue light in the two types of pixels that have high response in the blue, i.e., white and cyan pixels. This largest PRNU is a shading effect with a typical amplitude of 25% peak-to-peak. This compares with a typical shading PRNU in the basic CCD133 of 15% peak-to-peak. Other PRNU amplitudes are typically 15 to 20% peak-to-peak.

FIG. 2

RELATIVE RESPONSE SPECTRA OF THE CCD133K WITH AN EXTERNAL IR-BLOCKING FILTER (2mm BG-38)

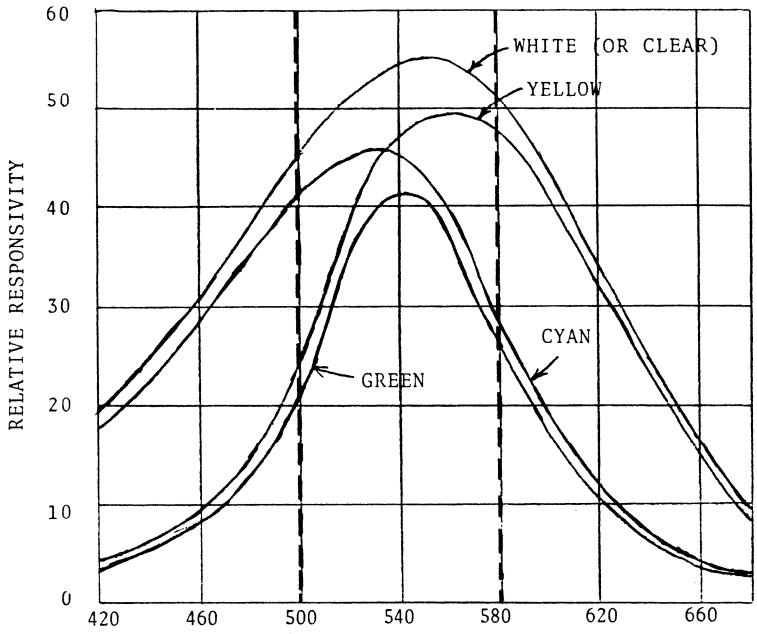


FIG. 3

THE DERIVED SIGNALS FROM THE CCD133K WHICH APPROXIMATE THE LUMINOSITY FUNCTION

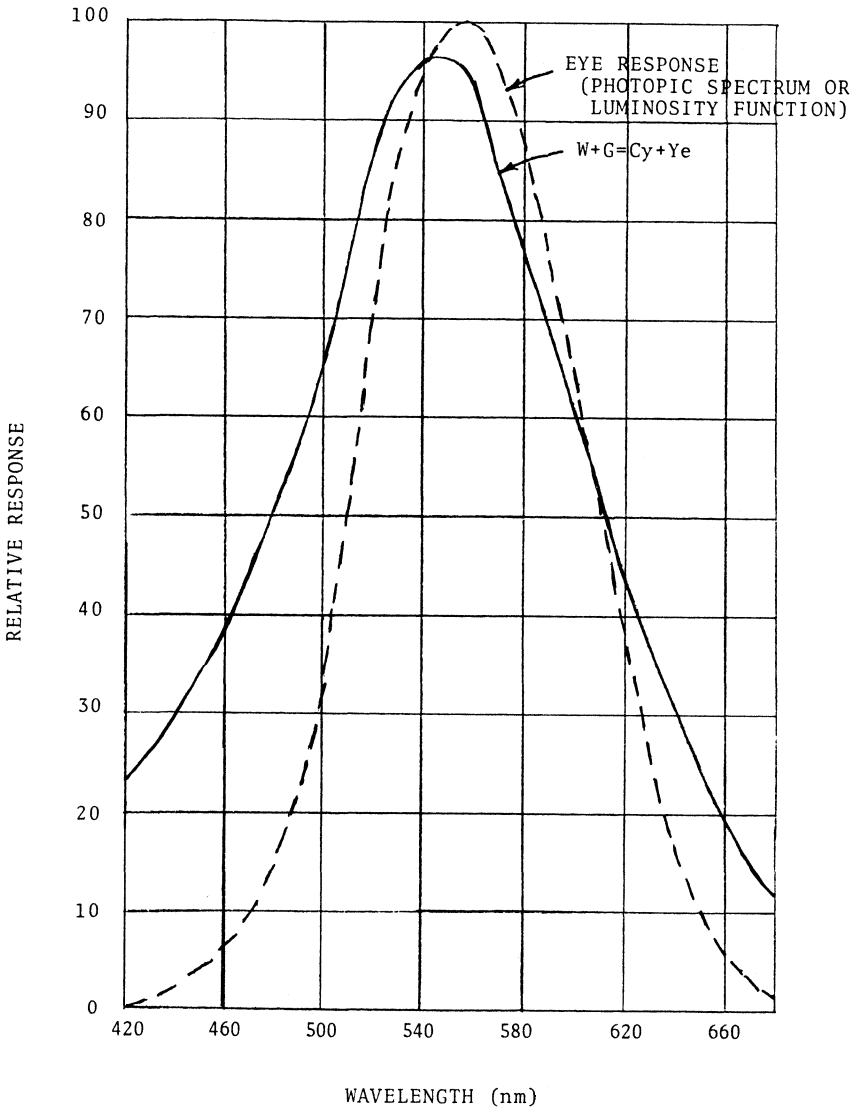


Table II

COLOR SIGNAL PROCESSING REQUIRED TO DERIVE LUMINANCE, RED AND BLUE SIGNALS

CHANNEL	PIXEL NUMBER	PIXEL COLOR	DERIVED LUMINANCE SIGNAL	DERIVED RED & BLUE SIGNAL
A	1	G		
B	2	W	G+W=L	
A	3	Ye		W-Ye=B
B	4	Cy	Ye+Cy=L	W-Cy=R
A	5	G		
B	6	W	G+W=L	
A	7	Ye		W-Ye=B
B	8	Cy	Ye+Cy=L	W-Cy=R
A	9	G		
B	10	W	G+W=L	
A	11	Ye		W-Ye=B
	etc.			

FAIRCHILD
A Schlumberger Company

CCD

CCD134
1024-Element
Line Scan Image Sensor

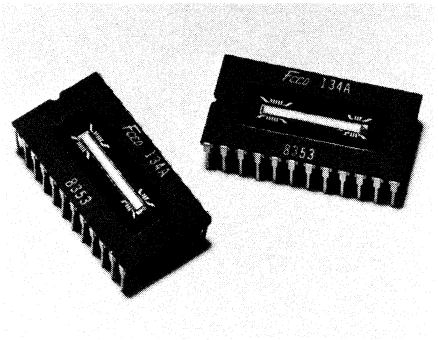
Preliminary

CCD Imaging

DESCRIPTION

The CCD134 is a 1024-element line image sensor designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolution, high sensitivity and high data rates. The incorporation of on-chip blooming and exposure controls allow the CCD134 to be extremely useful in an industrial measurement and control environment or environments where lighting conditions are difficult to control.

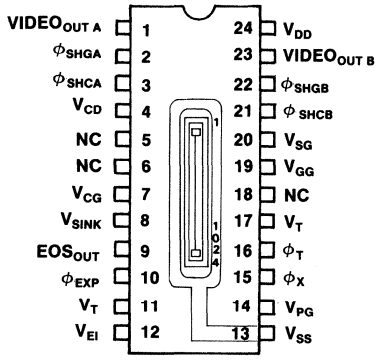
The CCD134 is similar to the CCD133 except for the additional features of blooming and exposure controls. The device incorporates on-chip clock driver circuitry and is capable of high-speed operation up to a 20MHz data rate. The photoelement size is 13μm (0.51 mils) by 13μm (0.51 mils) on 13μm (0.51 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.



FEATURES

- **BLOOMING AND EXPOSURE CONTROLS**
- **ENHANCED SPECTRAL RESPONSE (PARTICULARLY IN THE BLUE REGION)**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **ON-CHIP CLOCK DRIVERS**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1 PEAK-TO-PEAK OUTPUTS**
- **DARK AND WHITE REFERENCES CONTAINED IN SAMPLE-AND-HOLD OUTPUTS**
- **SINGLE POWER SUPPLY**

CONNECTION DIAGRAM
DIP (TOP VIEW)



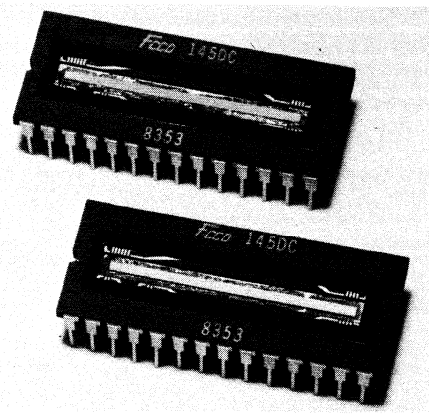
PIN NAMES

V_{PG}	Photogate
V_{GG}	Amplifier Bias
ϕ_X	Transfer Clock
ϕ_T	Transport Clock
ϕ_{EXP}	Exposure Clock
VIDEO$_{out\ A}$	Output Amplifier A Source
VIDEO$_{out\ B}$	Output Amplifier B Source
EOS_{out}	End-of-Scan Output
V_{DD}	Output Amplifier Drain
V_{CD}	Clock Driver Drain
V_{EI}	Electrical Input Bias
V_T	Transport Register DC Electrode
V_{SINK}	Blooming Control Sink
ϕ_{SHGA}	Sample-and-Hold Gate A
ϕ_{SHGA}	Sample-and-Hold Clock A
ϕ_{SHGB}	Sample-and-Hold Gate B
ϕ_{SHGB}	Sample-and-Hold Clock B
V_{CG}	Clock Ground
V_{SG}	Signal Ground
V_{SS}	Substrate Ground
NC	No Connection (Do not Ground)

CCD145
2048-Element
Line Scan Image Sensor

Preliminary

CCD Imaging



DESCRIPTION

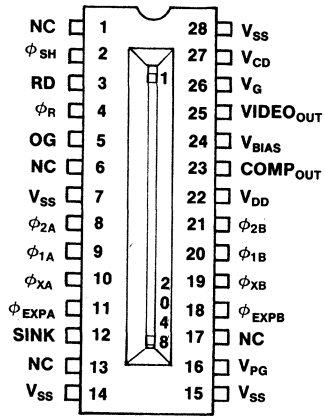
The CCD145 is a 2048-element line image sensor designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolutions, high sensitivity and high data rates. The incorporation of on-chip blooming and exposure controls allow the CCD145 to be extremely useful in industrial measurement and control environments or environments where lighting conditions are difficult to control.

The photoelement size is 13μm (0.51 mils) by 13μm (0.51 mils) on 13μm (0.51 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel Isoplanar buried-channel technology.

FEATURES

- **BLOOMING AND EXPOSURE CONTROLS**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1V PEAK-TO-PEAK OUTPUTS**
- **DARK REFERENCE CONTAINED IN A SAMPLE-AND-HELD OUTPUT**

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

V_{PG}	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Clocks
ϕ_{1A}, ϕ_{2A} ϕ_{1B}, ϕ_{2B}	Transport Clocks
ϕ_R	Reset Clock
ϕ_{SH}	Sample-and-Hold Clock
ϕ_{EXPA}, ϕ_{EXPB}	Exposure Clocks
$VIDEO_{OUT}$	Output Amplifier Source
$COMP_{OUT}$	Compensation Amplifier Source
V_{DD}	Output Amplifier Drain
V_{CD}	Compensation Amplifier Drain
RD	Reset Drain
OG	Output Gate
SINK	Blooming Control Sink
S_{BIAS}	Amplifier Bias
V_G	Amplifier Ground
V_{SS}	Substrate Ground
NC	No Conection (Do Not Ground)

FAIRCHILD
A Schlumberger Company

CCD

CCD151
3456 – Element
Line Scan Image Sensor

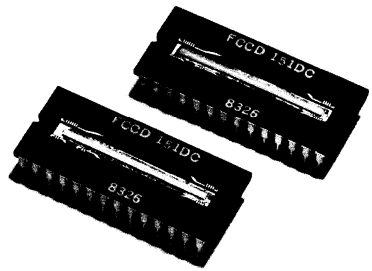
CCD Imaging

DESCRIPTION

The CCD151 is a 3456-element line image sensor designed for page scanning applications including facsimile, copier, optical character recognition and other imaging applications which require very high resolution, high sensitivity and high data rates.

The 3456 sensing elements of the CCD151 provide a 400-line per inch resolution across an 8½ inch page which is double the international facsimile standard and satisfactory for many copier applications.

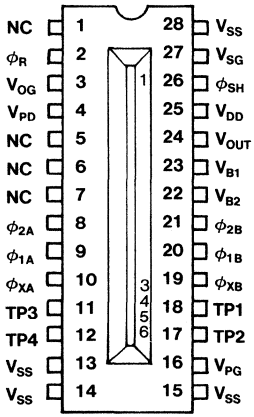
The photoelement size is 7μm (0.28 mils) by 7μm (0.28 mils) on 7μm (0.28 mils) centers. The device is manufactured using Fairchild advanced charge-coupled device n-channel isoplanar buried-channel technology.



FEATURES

- **VERY HIGH RESOLUTION: 3456 ELEMENTS**
- **SMALL ELEMENT PITCH: 7μm**
- **LOW DARK SIGNAL**
- **HIGH RESPONSIVITY**
- **DYNAMIC RANGE TYPICAL: 2500:1**
- **OVER 1V PEAK-TO-PEAK OUTPUT**
- **DARK REFERENCE CONTAINED IN SAMPLED-AND-HELD OUTPUT**

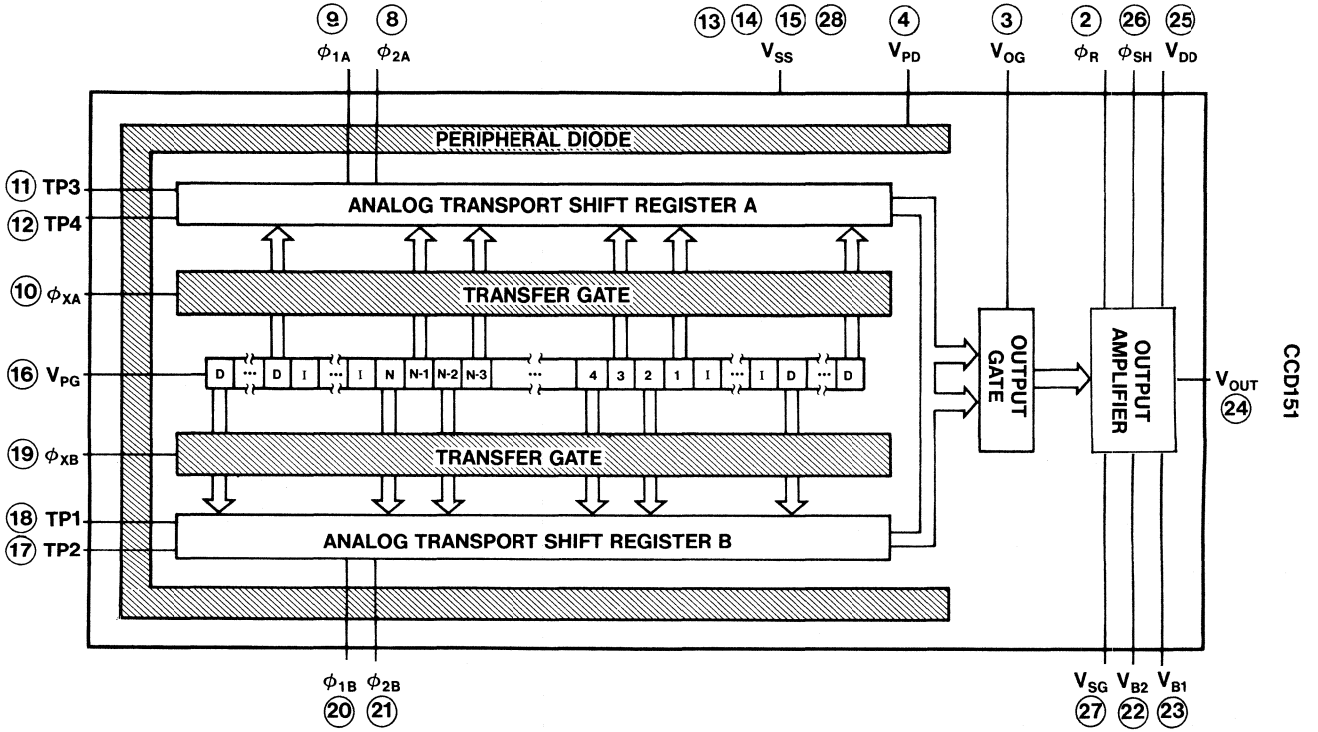
CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

V_{PG}	Photogate
ϕ_{XA}, ϕ_{XB}	Transfer Clocks
ϕ_{1A}, ϕ_{2A}	Transport Clocks
ϕ_{1B}, ϕ_{2B}	
V_{OG}	Output Gate
V_{OUT}	Video Output Terminal
V_{DD}	Output Amplifier Drain
V_{B1}	Output Amplifier Bias 1
V_{B2}	Output Amplifier Bias 2
ϕ_R	Reset Clock
ϕ_{SH}	Sample-and-Hold-Clock
V_{SG}	Signal Ground
V_{SS}	Substrate (Ground)
NC	No Connection
TP1, TP2	Test Points
TP3, TP4	
V_{PD}	Peripheral Diode

BLOCK DIAGRAM



○ = CCD 151 PIN NUMBER
D = DARK REFERENCE CELL
I = ISOLATION CELL
N = 3456 FOR CCD 151

CCD151

FUNCTIONAL DESCRIPTION

The CCD151 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 3456 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the A and B transport registers.

Two Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complimentary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output V_{OUT}. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Dark Reference Circuitry — Eight additional sensing elements at both ends of the array are covered by opaque metalization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the illuminated sensor elements (labeled "D" in the Block Diagram). These reference levels are useful as inputs to external dc restoration circuitry.

Peripheral Diode — Serves to reduce peripheral electron noise in the inner shift registers.

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Pixel — A picture element (photosite).

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Sample-and-Hold Clock ϕ_{SH} — The voltage waveform applied to the sample-and-hold gate in the output amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SH} to V_{DD}.

Gated Charge Detector/Amplifier — The output circuit of the CCD151 that receives the charge packets from the transport registers and provides a signal voltage proportional to the size of each charge packet received. Before each new charge packet is sensed, a reset clock returns the charge detector voltage to a fixed level.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external dc restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. (This does not take into account dark signal components.) Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

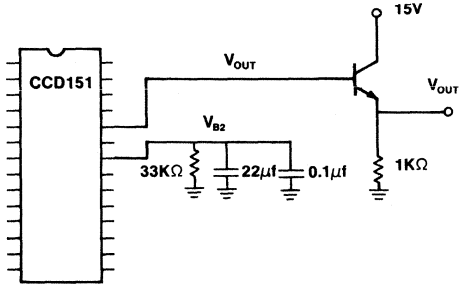
Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive elements under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature.

Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The integration time is the time between transfers of signal charge from the photosites into the transport registers.

TEST LOAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature (See Curves)	−25°C to +70°C
Pins 2, 3, 4, 8, 9, 10, 11, 12, 17, 18, 19, 20, 21, 22, 23, 25, 26, 27	−0.3 V to 18V
Pin 16	−0.3 V to 16V
Pins 13, 14, 15, 28	0V
Pins 1, 5, 6, 7 (See Caution Note)	NC
Pin 24 (See Caution Note)	Video Output

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting V_{OUT} to V_{SS}, or V_{DD} during operation of the devices. Shorting these pins even temporarily may destroy the output amplifiers.

Do not connect anything to a pin marked NC. They may be internally connected.

DC CHARACTERISTICS: $T_P = 25°$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN.	RANGE TYP.	RANGE MAX.	UNITS	NOTES
V_{DD}	Output Amplifier Drain Supply Voltage	14.5	15.0	15.5	V	
I_{DD}	Output Amplifier Drain Supply Current		5.0	16.1	mA	
V_{PG}	Photogate Bias Voltage	4.0	4.5	5.0	V	
V_{PD}	Peripheral Diode Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage	7.5	8.0	8.5	V	
V_{B1}	Output Amplifier Bias 1	4.5	5.0	5.5	V	
V_{B2}	Output Amplifier Bias 2					16
V_{SG}	Signal Ground		0.6		V	
V_{SS}	Substrate (Ground)		0.0		V	
TP1, TP3	Test Points	4.0	4.5	5.0	V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CLOCK CHARACTERISTICS: $T_P = 25°$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN.	RANGE TYP.	RANGE MAX.	UNITS	NOTES
$V_{Ø1AL}$, $V_{Ø1BL}$ $V_{Ø2AL}$, $V_{Ø2BL}$	Transport Clocks LOW	0.0	0.6	1.0	V	2, 3, 4
$V_{Ø1AH}$, $V_{Ø1BH}$ $V_{Ø2AH}$, $V_{Ø2BH}$	Transport Clocks HIGH	11.5	12.0	12.5	V	3, 4
$V_{ØXAL}$, $V_{ØXBL}$	Transfer Clocks LOW	0.0	0.6	1.0	V	2, 5
$V_{ØXAH}$, $V_{ØXBH}$	Transfer Clocks HIGH	11.5	12.0	13.5	V	5
$V_{ØRL}$	Reset Clock LOW	0.0	0.6	1.0	V	2, 6
$V_{ØRH}$	Reset Clock HIGH	11.5	12.0	12.5	V	6
$V_{ØSHL}$	Sample Clock LOW	0.0	0.6	1.0	V	2, 7
$V_{ØSHH}$	Sample Clock HIGH	11.5	12.0	12.5	V	7
$f_{ØR}$	Maximum Reset Clock Frequency (Output Data Rate)	2.5	5.0		MHz	8

CCD151

AC CHARACTERISTICS: T_P = 25° C, $f_{\phi R}$ = 1.0MHz, t_{int} = 4ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM filters.* All operating voltages nominal specified values. (Note 1)

SYMBOL	CHARACTERISTIC	RANGE MIN.	RANGE TYP.	RANGE MAX.	UNITS	NOTES
DR	Dynamic Range					
	(relative to rms noise)	500:1	2500:1			9
	(relative to peak-to-peak noise)	100:1	500:1			
NEE	RMS Noise Equivalent Exposure		.0001		$\mu J/cm^2$	10
SE	Saturation Exposure		.360		$\mu J/cm^2$	10, 11
CTE	Charge Transfer Efficiency		.99999		%	12
V_O	Output DC Level	4.0	5.5	7.5	V	
P	Power Dissipation		75	250	mW	
Z	Output Impedance		1.5	3.0	kΩ	
N	Peak-to-Peak Noise		4		mV	

PERFORMANCE CHARACTERISTICS: T_P = 25° C, $f_{\phi R}$ = 1.0MHz, t_{int} = 4ms, Light Source = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM filters.* All operating voltages nominal specified values. (Note 1)

SYMBOL	CHARACTERISTICS	RANGE MIN.	RANGE TYP.	RANGE MAX.	UNITS	NOTES
PRNU**	Photoresponse Non-uniformity					
	Peak-to-Peak		120	160	mV	
	Peak-to-Peak without Single-Pixel Positive and Negative Pulses		80		mV	
	Single-pixel Positive Pulses		70		mV	
	Single-pixel Negative Pulses		100		mV	
	Register Imbalance ("Odd"/"Even")		20		mV	
DS	Dark Signal					
	DC Component		.5	2	mV	13
	Low Frequency Component		.5	5	mV	13
SPDSNU	Single-pixel DS Non-uniformity		3	8	mV	14
R	Responsivity	3	4.0	9	Volts per $\mu J/cm^2$	10, 15
V_{SAT}	Saturation Output Voltage	1000	1800	3000	mV	

* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.

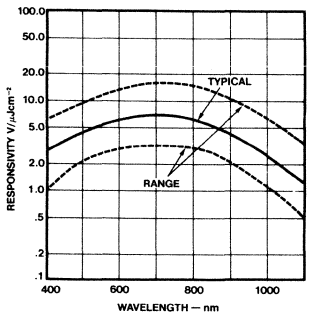
** All PRNU measurements are taken at an 800mV output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window aberrations to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

NOTES

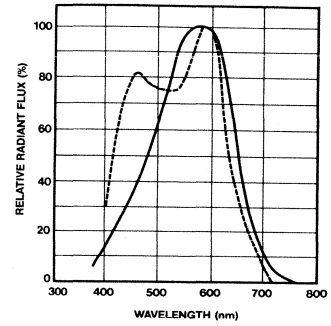
1. T_P is defined as the package temperature.
2. Negative transients on any clock pin going below 0.0V may cause charge injection which results in an increase of apparent DS.
3. $C_{\phi 1A,B}$ = 250pF.
4. $C_{\phi 2A,B}$ = 250pF.
5. $C_{\phi XA,B}$ = 250pF.
6. $C_{\phi R}$ = 5pF.
7. $C_{\phi SH}$ = 5pF.
8. Minimum clock frequency is limited by increase in dark signal.
9. Dynamic range is defined as V_{SAT}/Peak-to-Peak (temporal) or V_{SAT}/RMS Noise
10. 1 $\mu j/cm^2 \cong$ 42 lux-sec/cm^2 for the 2854°K source with 2.0mm Schott BG-38 and OCLI WBHM filters.
11. SE for 2854°K light without 2.0mm Schott BG-38 and OCLI WBHM filters is typically 0.42 $\mu j/cm^2$.
12. CTE is the measurement for a one-stage transfer.
13. Dark signal component approximately doubles for every 5–10°C increase in T_P, depending on the particular device.
14. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 5–15°C increase in T_P, depending on the particular device.
15. Responsivity for 2854°K source without 2.0mm Schott BG-38 and. OCLI WBHM filters typically 4.3 V/$\mu j/cm^2$.
16. See test load configurations. V_{B2} is created internally by loading Pin 22 as shown.

TYPICAL PERFORMANCE CURVES

TYPICAL SPECTRAL RESPONSE

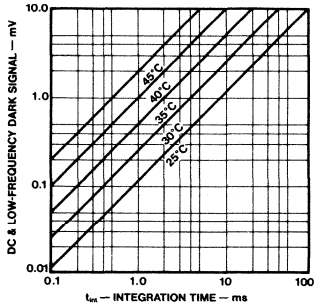


RELATIVE RADIANT FLUX VERSUS WAVELENGTH

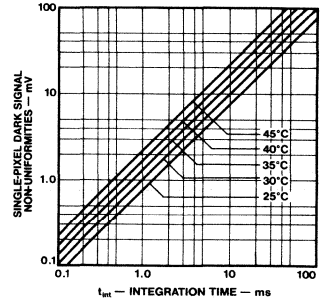


----- TYPICAL "DAYLIGHT FLUORESCENT" BULB
—— 2854° K LIGHT SOURCE + WBHM + 2.0 mm THICK BG-38

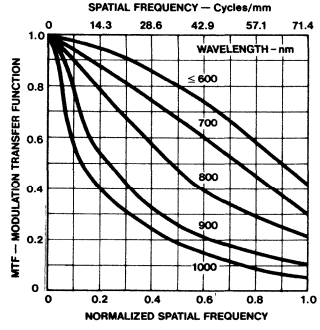
DC AND LOW-FREQUENCY DARK SIGNAL VERSUS INTEGRATION TIME



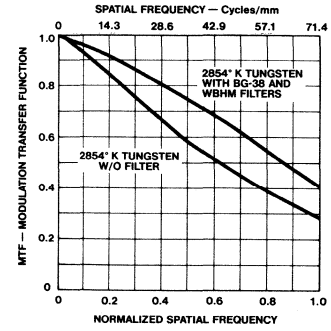
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



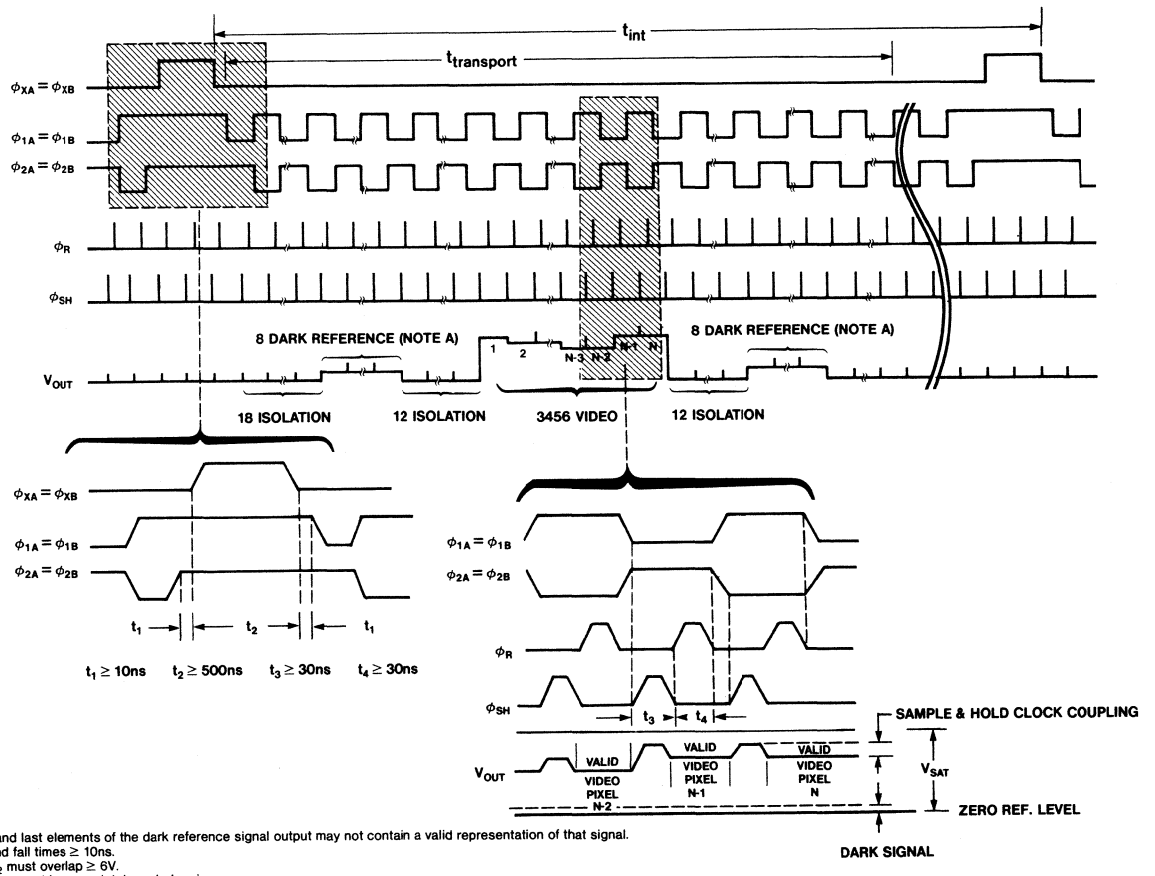
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



TIMING DIAGRAM

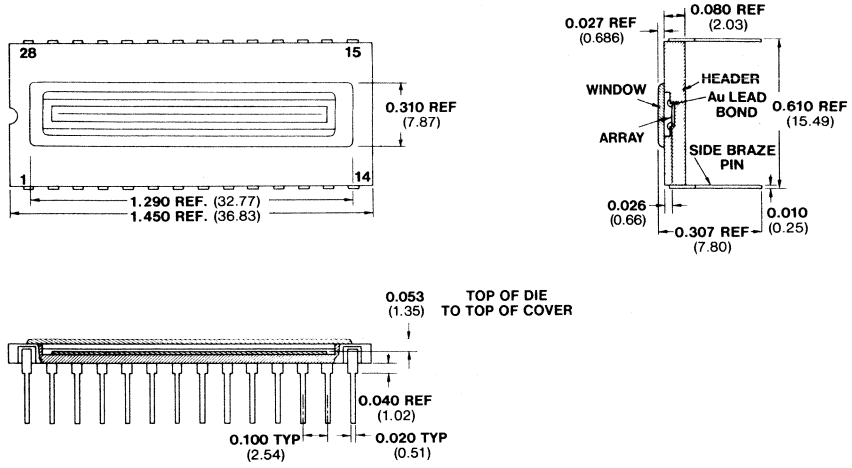


NOTES

A. The first and last elements of the dark reference signal output may not contain a valid representation of that signal.
B. All rise and fall times ≥ 10ns.
C. ϕ_1 and ϕ_2 must overlap ≥ 6V.
D. ϕ_R and ϕ_{SH} must be completely underlapping.
E. ϕ_R must occur entirely within the high time of the high ϕ_1 or ϕ_2 clock. ϕ_{SH} must occur entirely within the low time of the other transport clock.

CCD151

PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass. The amplifier of the device is located near the notched end of the package.

DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 12°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD151 DC where "D" stands for a ceramic package and "C" for commercial temperature range.

Also available separately is a printed circuit board that includes all the necessary clocks, logic drivers and video amplifiers to operate the CCD151DC. The board is fully assembled and tested and requires only one power supply for operation (+20V). The printed circuit board order code is: CCD151DB.

Description	Device Type Order Code
CCD151 3456×1 Line Image Sensor	CCD151DC
Design Development Board for CCD151	CCD151DB

CCD151 DESIGN DEVELOPMENT BOARD

SET-UP AND CIRCUIT DESCRIPTION

The Fairchild CCD151DB design development board is a design aid for the Fairchild CCD151 3456 element line scan image sensor. The board is fully assembled and tested, and requires only a plus 17V power supply (350 mA maximum current) and an oscilloscope to display the video information from the CCD sensor.

The CCD151 sensor is located in a socket on the back side of the board. The board I/O are made through a 22 position double readout edge card connector with 0.156 inch center-to-center finger spacings. It is provided with full freedom in choosing any of the four combinations of internal/external transport clock and internal/external exposure clocks. When connector fingers 17 and 6 are low, external phase clock and exposure clock can be fed in from fingers 5 and 3 respectively. To synchronize with a scope, the board provides exposure and phase clock outputs from fingers 7 and 9 respectively.

The positive side of the 20V power supply should be tied to pins 1 and A of the edge card connector, while the negative power supply lead is tied to ground through pins 22 and Z. There are three regulator IC's on the board, one supplying 5V (V_{CC}) to all TTL logic components, the other providing 15V (V_{CLK}) to the clock drivers and another supplying 15V (V_{DD}) to the CCD sensor and the video buffer, thus ensuring noise separation between digital and analog lines.

For self-contained operation, connector pins 17 and 6 are left open. This enables the internal transport clock (ϕ clock) and exposure clock (both from U1) out of pins 7 and 9 of U12. Series connected inverters U7 and U9 serve as tapped delay line and, with two exclusive OR gates in U13, produce the sample/hold (S/H) and the reset pulses. The following gates (two EXOR and four inverters) provide sufficient separation between the reset pulse and the transport clocks (ϕ_1, ϕ_2) and control the cross-over of ϕ_1 and ϕ_2. Hex 74LS14 Schmitt trigger inverters are used for U8 to give sufficient S/H and reset pulse separation through the inverter at pins 11 and 10. For those users who wish to operate at high data rates, the reset pulse width can be narrowed by jumping over two out of the seven reset-pulse inverters (in U8, U7) at a time. Typical clock waveforms are shown in Figure 1.

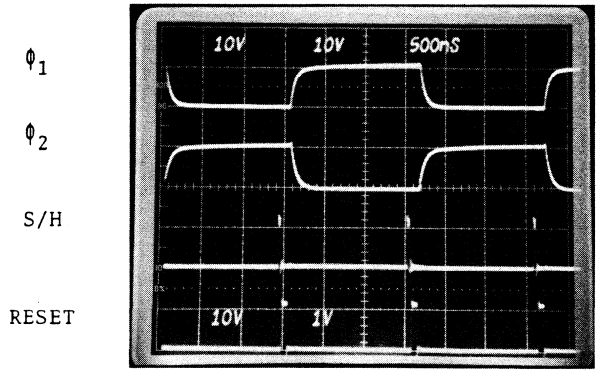


FIGURE 1 TYPICAL CLOCK WAVEFORMS (I) TAKEN AT SENSOR TERMINALS.

The transport clock frenquency can be varied by potentiometer VR1 at the top of the board from 280KHz to 2.3MHz. The exposure clock can be varied from 60Hz to 360Hz with potentiometer VR2. Users can increase or decrease the clock frequency range by replacing C_5 or C_6 with smaller or larger-value capacitors.

The exposure clock from pin 9 of U2 is synchronized with ϕ_2 in U4. U2 produces sufficient pulse width for ϕ_X, and U4 supplies a wider pulse to stop ϕ_1 and ϕ_2 at the high level from one clock before to one clock after ϕ_X. U11 and U13 translate TTL clock levels to the 14 volt swing recommended for the CCD151. The diodes and resistors between drivers and sensor serve as precaution against the possibility of charge injection inside the sensor due to too fast slew rate on the clocks, or due to clocks going below the substrate voltage level (which is tied to the ground). "Dynamic damping" is performed by head-to-tail parallel-connected diodes that their effective resistance are varied with the amount of charging current from driver to sensor. The charging current decreases when clock waveform approaches either high or low level. Waveform ringings are thus effectively suppressed by the increasing diode resistance. These dynamic damping diodes also assure that clocks at the sensor terminals are one diode drop above ground in the low level. Figure 2 shows exposure pulse related to ϕ_1, ϕ_2 and reset pulses.

ϕ_1

ϕ_2

ϕ_X

RESET

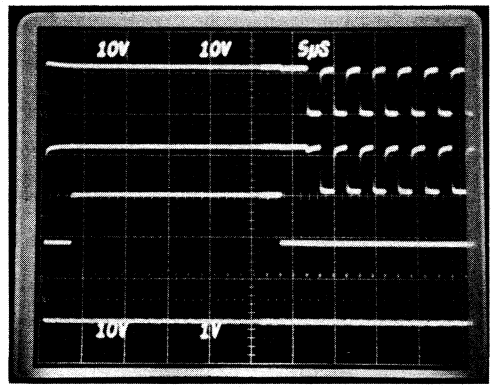
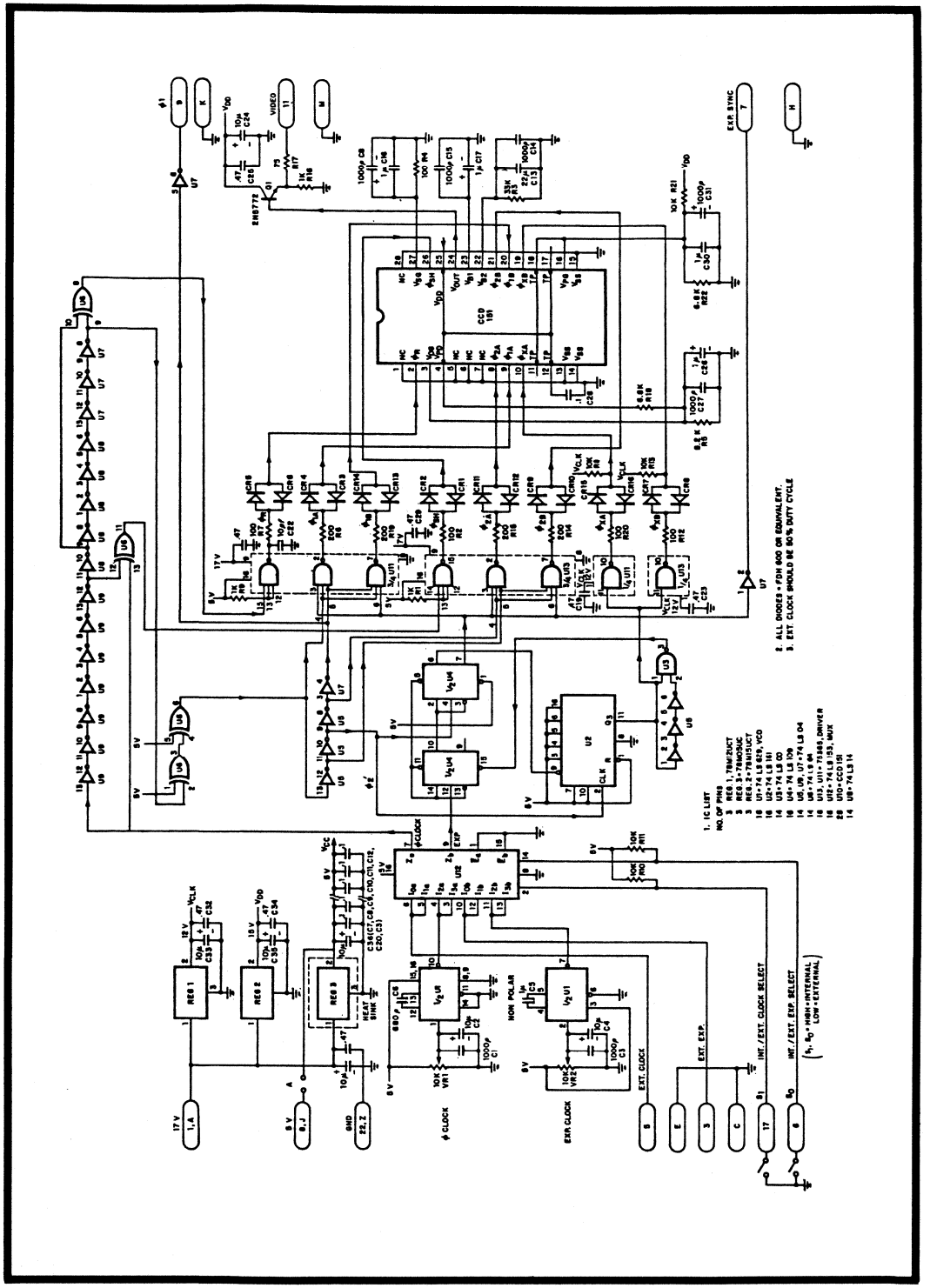


FIGURE 2 TYPICAL CLOCK WAVEFORMS (II) SHOWING RELATIONS BETWEEN ϕ_X AND ϕ_1, ϕ_2 AND RESET PULSES.



CCD IMAGING AND SIGNAL PROCESSING

Signal Processing Products

IMAGING

The capability to manipulate information in the form of discrete charge packets makes CCD technology ideal for analog signal processing.

Fairchild signal processing components are monolithic silicon structures comprised of CCD analog shift registers, charge injection ports, and output charge-sensing amplifiers. They can be advantageously used for delay and temporary storage of analog video signals. The time delay for data transit through the CCD register is precisely controlled by the frequency of the externally supplied transport clock signal. Fairchild signal processing components include a sample-and-hold signal output stage for ease of application.

Fairchild video delay modules are printed circuit board structures which include the CCD321A2 device and are sold as fully assembled and calibrated units. The module is equipped for use as a variable delay circuit, using either an externally supplied or internal variable frequency clock, or for temporary analog data storage in a stopped-clock mode.

Typical applications for the CCD signal processing components and modules include time base correction for video tape recorders, fast input-slow output data expansion systems for A-D converter systems, comb filter realizations, drop-out compensators, and other analog applications up to frequencies of 30 MHz data rate.

CCD321A Variable Analog Delay Line 455/910 Bit

Th CCD321A is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321A consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

The CCD321A can be used in applications ranging from video frefrequencies to audio frequencies. A complete TV line of 63.5 μs can be stored with a sampling frequency of 14.318 MHz (four times color subcarrier frequency of 3.58 MHz). Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321A also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.

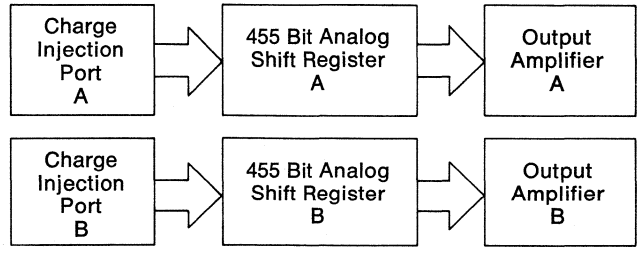
The CCD321A is available in four different classes as follows:

Device	Application
CCD321A-1	Broadcast quality video delay line
CCD321A-2	Industrial video delay line
CCD321A-3	Time base compression and expansion delay line
CCD321A-4	Audio delay line

CCD321A Features

- Electrically variable analog delay line for audio and video applications.
- 1 H video delay line capability with broadcast quality performance.
- Excellent bandwidth at video and audio rates due to buried channel technology.
- Wide range of data rate: From 10 kHz to 20 MHz per 455 section.
- High signal to noise ratio — Video: 58 dB, Audio: 65 dB.

CCD321A — Block Diagram



FAIRCHILD
A Schlumberger Company

CCD

IMAGING

Signal Processing Products

CCD323A Video Delay Line With On-Chip Drivers 283 ½-Bit

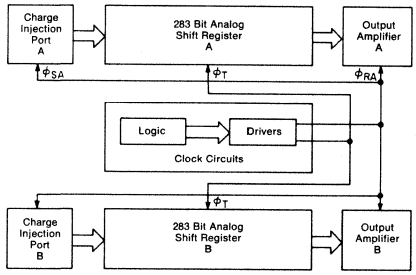
The CCD323A is a 283 ½-bit, dual channel, high speed video delay line with on-chip clock drivers and logic circuits greatly simplifying external circuit design. Only one TTL level clock is required by the user to operate the device, thereby saving many external components as well as board space.

With 283 ½-bits length and clocking done at ≅4.4 MHz, the device produces a delay of ≅64 μsec. to ideally suit PAL TV applications. However, the device is useful in many high speed applications using a delay line shorter than the CCD321A.

CCD323A Features

- Electrically variable analog delay line.
- 64 μsec. at 4.4 MHz clock rate (PAL TV).
- On-chip clock circuits. Requires one external clock. Simplifies external circuit design.
- Excellent bandwidth at video data rates due to buried channel technology.
- Wide range of data rates: From 10 kHz to 15 MHz.
- High signal to noise ratio.

CCD323A — Block Diagram



CCD321M Video Delay Module

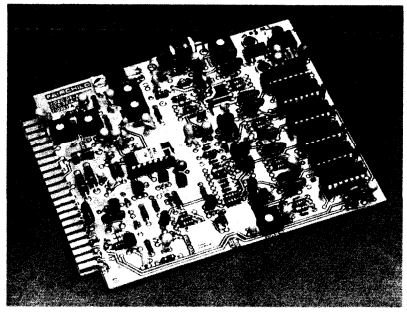
The CCD321M is a complete delay module intended for use in video signal processing systems where precisely controlled delay or temporary storage of analog information is required. The module is a printed circuit board containing a Fairchild CCD321 dual 455-bit analog shift register, input and output signal processing circuitry, and the required clocking signal sources and bias voltage controls. The module requires a single +20 V power supply input for operation.

The delay time of analog signals through the CCD321M is precisely controlled by the clock signal frequency which can be provided by an external source or obtained from an internal VCO. The CCD321M can be used as a 910-bit one horizontal line (1 H) delay for TV video bandwidths of 5 MHz when operating with a 4 × 3.58 = 14.3 MHz clock frequency, serve as a temporary analog store for a full-bandwidth TV line, or can be used as an adjustable delay by controlling either the internally generated or external input clock. The CCD321M can also be used as two 455-bit registers for delay of two independent analog signals.

Typical video applications for the CCD321M include time-base correctors, video re-synchronizing systems, comb filter realizations, moving target indicators and signal-to-noise enhancement systems. Other applications include time-base compression and expansion systems, phase delay equalizers and general purpose analog delay.

CCD321M Features

- 1 H delay line performance
- Electrically variable delay
- Adjustable delay—by clock control
- Wide signal bandwidth — 5 MHz
- High S/N ratio — 55 dB
- Dual 455-bit or single 910-bit delay
- No drift — delay dependent on clock frequency
- Internal or external clocking
- Temporary storage operation controlled by a single TTL input line
- Single polarity power supply — +20 V



CCD321A

455/910—BIT ANALOG SHIFT REGISTER

CHARGE COUPLED DEVICE

GENERAL DESCRIPTION—The CCD321A is an electrically variable analog delay line intended to be used in analog signal processing systems that include delay and temporary storage of analog information. The CCD321A consists of two 455-bit analog shift registers, each with its own charge injection port, transport clock and output port allowing the device to be used as two 455 or one 910-bit analog delay line.

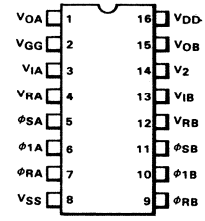
The CCD321A can be used in applications ranging from video frequencies to audio frequencies. A complete TV line of 63.5 μs can be stored with a sampling frequency of 14.318 MHz (four times color subcarrier frequency of 3.58 MHz). Applications in video systems include time base correction, comb filtering and signal-to-noise enhancing. Audio applications include variable delay of audio signals, reverberation effects in stereo equipment, tone delay in organs and musical instruments as well as voice scrambling applications. The CCD321A also finds applications in time base compression and expansion applications where analog data can be fed at one rate to the device, the clocks can be temporarily stopped and then data clocked out at a different rate.

The CCD321A is an improved pin-for-pin replacement for the CCD321. The CCD321A is available in four different classes as follows:

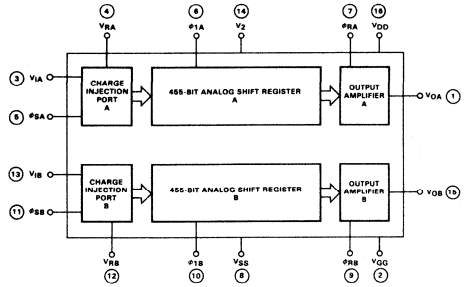
DEVICE	APPLICATION
CCD321A-1	Broadcast quality video delay line
CCD321A-2	Industrial video delay line
CCD321A-3	Time base compression and expansion delay line
CCD321A-4	Audio delay line

- **ELECTRICALLY VARIABLE ANALOG DELAY LINE FOR AUDIO AND VIDEO APPLICATIONS**
- **1 H VIDEO DELAY LINE CAPABILITY WITH BROADCAST QUALITY PERFORMANCE.**
- **EXCELLENT BANDWIDTH AT VIDEO AND AUDIO RATES DUE TO BURIED CHANNEL TECHNOLOGY.**
- **WIDE RANGE OF DATA RATE: FROM 10 kHz TO 20 MHz PER 455 SECTION.**
- **HIGH SIGNAL TO NOISE RATIO — VIDEO: 58 dB, AUDIO: 65 dB.**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES	
Φ_{1A},Φ_{1B}	Analog Shift Register Transport Clocks
Φ_{SA},Φ_{SB}	Input Sampling Clocks
Φ_{RA},Φ_{RB}	Output Sample and Hold Clocks
V_2	Analog Shift Register DC Transport Phase
V_{IA},V_{IB}	Analog Inputs
V_{RA},V_{RB}	Analog Reference Inputs
V_{OA},V_{OB}	Analog Outputs
V_{DD}	Output Drain
V_{GG}	Signal Ground
V_{SS}	Substrate Ground

FAIRCHILD CHARGE COUPLED DEVICE • CCD321A

FUNCTIONAL DESCRIPTION — The CCD321A consists of the following functional elements illustrated in the Block Diagram:

Two Charge Injection Ports — The analog information in voltage form is applied to two input ports at V_{IA} (or V_{IB}). Upon the activation of the analog sample clocks ϕ_{SA} (or ϕ_{SB}) a charge packet linearly dependent on the voltage difference between V_{IA} and V_{RA} (or V_{IB} and V_{RB}) is injected into analog shift register A (or B).

Two 455-Bit Analog Shift Registers — Each register transports the charge packets from the charge injection port to its corresponding output amplifier. Both registers are operated in the 1-1/2 phase mode where one phase (ϕ_{1A} or ϕ_{1B}) is a clock and the other phase (V_2) is an intermediate dc potential. Phases ϕ_{1A} and ϕ_{1B} are completely independent. V_2 is a dc voltage common to both registers.

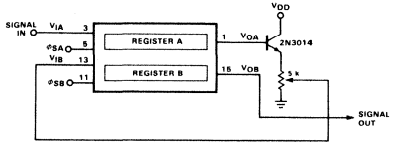
Two Output Amplifiers – Charge packets from each analog shift register are delivered to their corresponding output amplifier as shown in the circuit diagram. Each output amplifier consits of three source follower stages with constant current source bias. A sample and hold transistor is located between the second and third stage of the amplifier. When the gate of the sample and hold transistor is clocked (ϕ_{RA} or ϕ_{RB}) a continuous output waveform is obtained as shown in the timing diagrams. The sample and hold transistor can be defeated by connecting ϕ_{RA} and/or ϕ_{RB} to V_{DD}. In this case the output is a pulse modulated waveform as shown in the timing diagram.

MODES OF OPERATION — The CCD321A can be operated in four different modes:

455-Bit Analog Delay — Either 455-bit analog shift register can be operated independently as a 455-bit delay line. The driving waveforms to operate shift register A is shown in Fig. 10. The input voltage signal is applied directly to V_{IA}. The input sampling clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of register A. The input voltage A_1 which is sampled between $t = 0$ and $t = t_c$ appears at the output terminal V_{OA} @ $t = 910t_c$. If the sample and hold circuit is not used then the output appears as a pulse amplitude modulated waveform as shown in the diagram. In that case ϕ_{RA} (pin 7) should be connected to V_{DD} (pin 16). If the sample and hold circuit is used than the output appears as a continuous waveform. Here ϕ_{RA} (pin 7) should be clocked coincident with ϕ_{SA} (pin 5) and the two pins can be connected together.

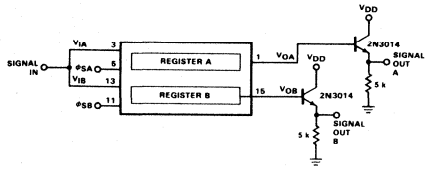
Analog shift register B can be operated in an analogous manner with V_{IB} as the analog input, ϕ_{1B} as the transport clock, ϕ_{SB} as the input sampling clock and ϕ_{RB} as the output sample and hold clock.

910-Bit Analog Delay In Series Mode — The two analog shift registers A and B can be connected in series to provide 910 bits of analog delay as shown in the schematic below. The analog signal input voltage is applied to V_{IA}. The output of register A is connected to the input of register B with a simple emitter follower buffer stage. In order to insure proper charge injection of register B, V_{RB} should be adjusted. The timing diagram shown in Fig. 10 applies in this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{SA} = \phi_{SB}$, $\phi_{RA} = V_{DD}$, and ϕ_{RB} is clocked.



910-Bit Analog Delay In Multiplexed Mode — The two analog shift registers can be connected in parallel to provide 910-bit of analog delay as shown in the schematic below. The analog signal input voltage is applied to both V_{IA} and V_{IB}. The outputs at V_{OA} and V_{OB} can be combined as shown in Fig. 8 to recover the analog input information.

The necessary waveforms to operate the device in this mode is shown in Fig. 11. In this case ϕ_{SA} samples the analog input A_1 at V_{IA} between $t = 0$ and $t = t_c$. ϕ_{SB} samples the analog input B, at V_{IB}, between $t = t_c$ and $t = 2t_c$. The output corresponding to A_1 appears at V_{OA} at $t = 910t_c$. The output corresponding to B_1 appears at V_{OB} @ $t = 911t_c$. This mode of operation results in an effective sampling rate of twice the rate of ϕ_{1A}, ϕ_{1B}, ϕ_{SA} and ϕ_{SB}.



Stop/Start Mode Operation — The charge packets in the two analog shift registers can be held stationary by stopping ϕ_{1A} and ϕ_{1B} in their LOW state. ϕ_{SA}, ϕ_{SB}, ϕ_{RA}, and ϕ_{RB} can also be stopped in the LOW state or kept clocking as usual. The two shift registers should not be connected in series in the stop-start mode of operation.

The CCD321A is available in four different classes for different applications. The CCD321A-1 is a high quality broadcast 1H delay line for video systems with 1% differential gain and 1° differential phase. The CCD321A-2 is a high quality video delay line with 3% differential gain and 3° differential phase. The CCD321A-3 is tested in the START/STOP mode of operation and parameters are guaranteed in this mode. The CCD321A-4 is tested at audio speeds; audio parameters are specified and guaranteed. The dc and clock characteristics of the four classes are the same. The ac characteristics vary as shown below.

Caution: The device has limited built-in gate protection. Charge build-up should be minimized. Care should be taken to avoid shorting pins V_{OA} and V_{OB} to ground during operation of the device.

DC CHARACTERISTICS: T_A = 55°C, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{DD}	Output Drain Voltage	14.5	15.0	15.5	V	
V_2	Analog Shift Register DC Transport Phase Voltage		6.0		V	Note 1
V_{RA}, V_{RB}	Analog Reference Inputs Voltage		3-7		V	Note 2
V_{GG}	Signal Ground		0.0			
V_{SS}	Substrate Ground		0.0			Note 3
V_{IA}, V_{IB}	Input DC Level		3-7		V	Note 2
V_{OA}, V_{OB}	Output DC Level		6-11		V	V_{DD} = 15 V
R_{IN}	Small Signal Input Resistance		1.0		MΩ	Resistance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V
C_{IN}	Small Signal Input Capacitance		10		pF	Capacitance from Pins 3, 4, 12 or 13 to V_{SS}. V_{IA} = V_{IB} = 3 V
R_{OUT}	Small Signal Output Resistance		250		Ω	V_{DD} = 15 V
ODM	Output DC Mismatch Between A & B Registers		±1		V	
OAM	Output AC Mismatch Between A & B Registers		±20		%	

CLOCK CHARACTERISTICS: T_A = 55°C, Note 16

SYMBOL	CHARACTERISTICS	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V\phi_{1AL}$, $V\phi_{1BL}$	Analog Shift Register Transport Clocks LOW	0	0.5	0.8	V	Note 4
$V\phi_{1AH}$, $V\phi_{1BH}$	Analog Shift Register Transport Clocks HIGH	12.0	13.0	15.0	V	Note 4
$V\phi_{SAL}$, $V\phi_{SBL}$	Input Sampling Clocks LOW	0	0.5	0.8	V	Note 5
$V\phi_{SAH}$, $V\phi_{SBH}$	Input Sampling Clocks HIGH	12.0	13.0	15.0	V	Note 5
$V\phi_{RAL}$, $V\phi_{RBL}$	Output Sample and Hold Clocks LOW	0	0.5	0.8	V	Note 6
$V\phi_{RAH}$, $V\phi_{RBH}$	Output Sample and Hold Clocks HIGH	12.0	13.0	15.0	V	Note 6
$f\phi_{1A}$, $f\phi_{1B}$	Analog Shift Register Transport Clock Frequency	0.02		20	MHz	See Note 17
$f\phi_{SA}$, $f\phi_{SB}$	Input Sampling Clocks Frequency	0.02		20	MHz	See Note 17
$f\phi_{RA}$, $f\phi_{RB}$	Output Sample and Hold Clocks Frequency	0.02		20	MHz	See Note 17

FAIRCHILD CHARGE COUPLED DEVICE • CCD321A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
All Pins with Respect to V_{SS}	−0.3 V to 18 V

CCD321A-1 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz. Sampling Rate = 14.32 MHz. Vout ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	5.0			MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			1.0	%	Note 9
Δ ϕ	Differential Phase			1.0	degree	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-2 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplexed mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Vout ≅ 700 mV. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	58			dB	Note 10
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-3 AC CHARACTERISTICS: T_A = 55°C. Both registers in the multiplied mode, Clock Rate = 7.16 MHz, Sampling Rate = 14.32 MHz. Clocks are stopped for 300 μs. Vout ≅ 700 mV after 4.2 MHz low pass filter. (See Test Load Configuration, Figure 8)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	4.2	5.0		MHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
Δ G	Differential Gain			3.0	%	Note 9
Δ ϕ	Differential Phase			3.0	degrees	Note 9
S/N	Signal-to-Noise Ratio	55			dB	Note 10
SN	Spacial Noise		10.0	20.0	mV	Notes 11, 12
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	

CCD321A-4 AC CHARACTERISTICS: $T_A = 45°C$. For each register, Data Rate = 50 KHz. (See Test Load Configuration, Figure 9)
Vout ≅ 1 V

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
BW	Signal Bandwidth (3 dB Down)	23	25		kHz	Note 7
IG	Insertion Gain	0	3.0	6.0	dB	Note 8
THD	Total Harmonic Distortion		0.5	1.0	%	Note 13
S/N	Signal-to-Noise Ratio	60	65		dB	Note 14
$V_{I\ (max)}$	Maximum Input Signal Voltage		1.0		V_{pk-pk}	
RSO	Rate of Average Signal Offset		15		mv/ms	Note 15

NOTES:
1. V_2 level should be 1/2 of the ϕ_{1A} or ϕ_{2A} HIGH level. Adjustment in the range of ±1 V may be necessary to maximize signal bandwidth.
2. Signal charge injection is proportional to the difference V_I and V_R. Adjustment of either V_I or V_R is necessary to assure proper operation.
3. Negative transients below ground of fast rise and fall times of the clocks may cause charge injection from substrate to the shift registers. Anegative bias on V_{SS} of -2.0 to -5.0 Vdc will eliminate the injection phenomenon.
4. $C_{\phi 1A} = C_{\phi 1B}$ = 30 pF = Capacitance with respect to V_{SS}.
5. $C_{\phi SA} = C_{\phi SB}$ = 10 pF = Capacitance with respect to V_{SS}.
6. $C_{\phi RA} = C_{\phi RB}$ = 10 pF = Capacitance with respect to V_{SS}.
7. Signal Bandwidth is typically 1/3 to 1/2 of the sampling rate. See Fig. 1.
8. Insertion Gain = 20 Log V_{OUT}/V_{IN}.
9. Differential Gain and Differential Phase are measured with Tektronix NTSC Signal Generator (147A) and Vector Scope (520A). See Figure 2.
10. Video S/N is defined as the ratio the peak-to-peak output signal to RMS random (temporal) noise. The peak-to-peak signal is the maximum output level that satisfies the ΔG and Δφ specs. See Fig. 3.
11. In the start/stop mode of operation is recommended that the rise and fall times of ϕ_{1A} and ϕ_{1B} exceed 20 ns to eliminate charge injection.
12. Spacial Noise is the peak-to-peak spacial variation (fixed pattern noise) in the device output after clocks have been stopped. It is usually caused by the variation of leakage current density in the shift registers. Spacial noise is a function of the clock stop period and temperature. See Figure 5.
13. Input Signal = 1 kHz sine wave. See Figure 6.
14. Audio S/N is defined as the ratio of RMS signal to RMS noise at 23 kHz bandwidth. Both are measured with an HP3400A RMS Voltmeter. See Figure 6.
15. Rate of Average-Signal Offset is caused by leakage current in the registers. It is function of temperature. See Figure 7.
16. Devices are tested using the values shown in the typical columns.
17. Devices can be operated beyond 20 MHz without damage. The minimum clock rate can be lower than 10 kHz as shown in Figure 4.

TYPICAL VIDEO PERFORMANCE CURVES

FREQUENCY RESPONSE (FOR SINGLE REGISTER)

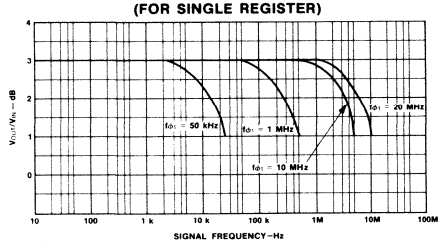


Fig. 1

DIFFERENTIAL GAIN AND PHASE VERSUS OUTPUT VOLTAGE

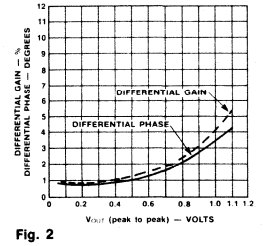


Fig. 2

DIFFERENTIAL GAIN AND PHASE VERSUS S/N RATIO

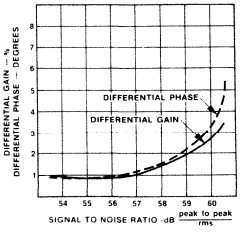


Fig. 3

VOUT MAX VERSUS CLOCK FREQUENCY

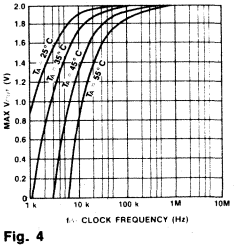


Fig. 4

SPACIAL NOISE VERSUS CLOCK STOP PERIOD

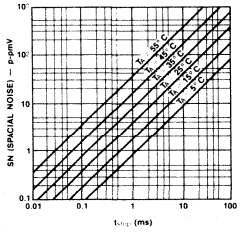


Fig. 5

FAIRCHILD CHARGE COUPLED DEVICE • CCD321A

TYPICAL AUDIO PERFORMANCE CURVES

TOTAL HARMONIC DISTORTION (THD) AND S/N RATIO VERSUS V_{OUT}

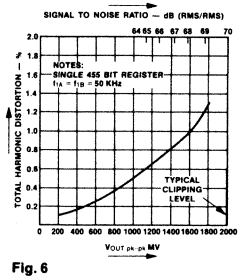


Fig. 6

RATE OF AVERAGE SIGNAL OFFSET VERSUS TEMPERATURE

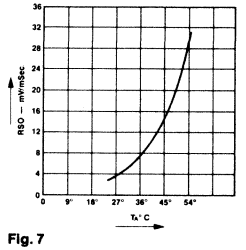


Fig. 7

TEST LOAD CONFIGURATION FOR MILTIPLEXED OPERATION IN VIDEO

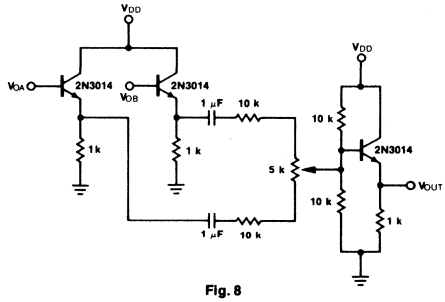


Fig. 8

TEST LOAD CONFIGURATION FOR SINGLE REGISTER OPERATION IN AUDIO AND VIDEO

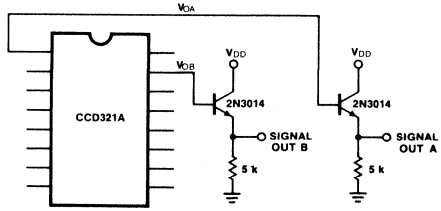
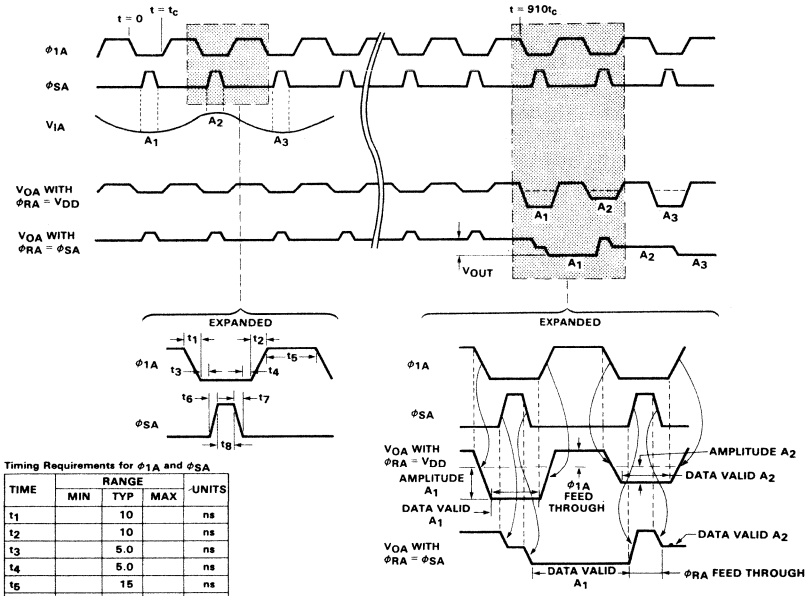


Fig. 9

TIMING DIAGRAM



Timing Requirements for ϕ_{1A} and ϕ_{SA}

TIME	RANGE MIN	RANGE TYP	RANGE MAX	UNITS
t_1		10		ns
t_2		10		ns
t_3		5.0		ns
t_4		5.0		ns
t_5		15		ns
t_6		5.0		ns
t_7		5.0		ns
t_8		5.0		ns

NOTE:
This timing diagram also applies for shift register B. In this case, ϕ_{1A} becomes ϕ_{1B}, ϕ_{SA} becomes ϕ_{SB}, V_{IA} becomes V_{IB} and V_{OA} becomes V_{OB}

Fig. 10 Analog Shift Register A or B Operation

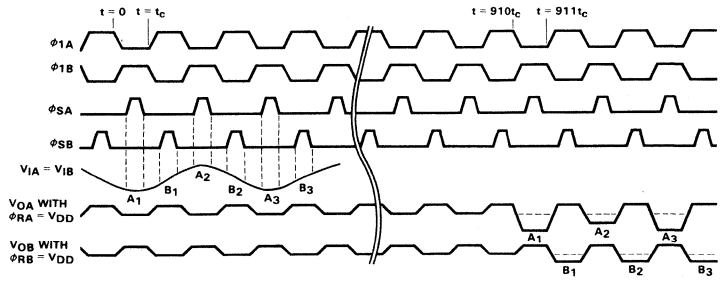
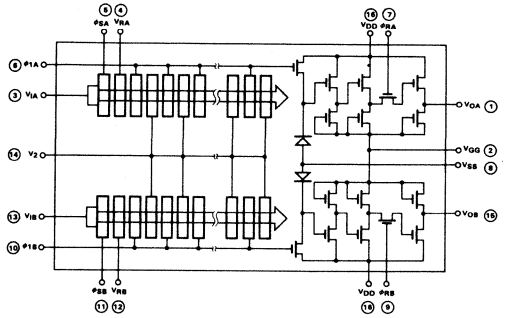


Fig. 11 Analog Shift Register A and B Operation in the Multiplexed Mode

FAIRCHILD CHARGE COUPLED DEVICE • CCD321A

Fig. 12 Circuit Diagram



ORDERING INFORMATION

To order the CCD321A specify the "device type" as shown below:

CLASS, APPLICATION	DEVICE TYPE
CCD321A-1, Broadcast quality video	CCD321A1
CCD321A-2, Industrial quality video	CCD321A2
CCD321A-3, Time base compression and expansion	CCD321A3
CCD321A-4, Audio delay line	CCD321A4

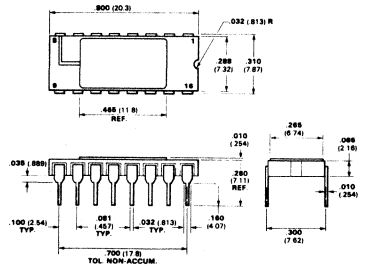
Also available from Fairchild is a fully-assembled module that contains all the necessary circuitry to operate the CCD321A. The module is designed to help the system designer become familiar with the operation of the device, and for use in OEM systems.

The CCD321VM is a video module using a CCD321A-3. The module includes the necessary electronics to perform time base compression and expansion, and variable video signal delay. The module requires a single power supply for operation.

Schematics and component layouts are included in the shipping packages for the CCD321VM. For further information on the CCD321VM please contact your nearest Fairchild sales office or distributor or call 415-962-3941.

PACKAGE OUTLINE

16-Pin Side Brazed



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Header is black ceramic (Al_2O_3)
Pins are gold-plated kovar
Top cover connected to pin 8 (V_{SS} substrate)

CCD321M

VIDEO DELAY MODULE

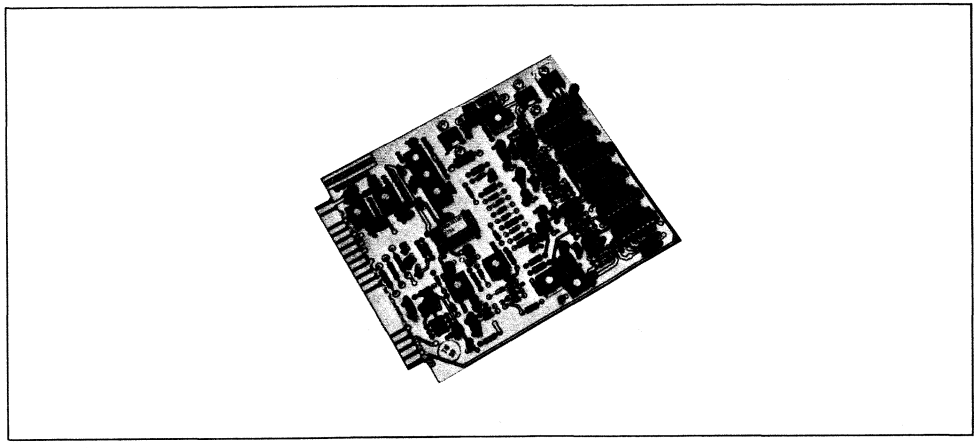
CHARGE COUPLED DEVICE

GENERAL DESCRIPTION – The CCD321M is a complete delay module intended for use in video signal processing systems where precisely controlled delay or temporary storage of analog information is required. The module is a printed circuit board containing a Fairchild CCD321 dual 455-bit analog shift register, input and output signal processing circuitry, and the required clocking signal sources and bias voltage controls. The module requires a single +20 V power supply input for operation.

The delay time of analog signals through the CCD321M is precisely controlled by the clock signal frequency which can be provided by an external source or obtained from an internal VCO. The CCD321M can be used as a 910-bit one horizontal line (1H) delay for TV video bandwidths of 5 MHz when operating with a 4 X 3.58 = 14.3 MHz clock frequency,serve as a temperary analog store for a full-bandwidth TV line, or can be used as a adjustable delay by controlling either the internally generated or external input clock. The CCD321M can also be used as two 455-bit registers for delay of two independent analog signals.

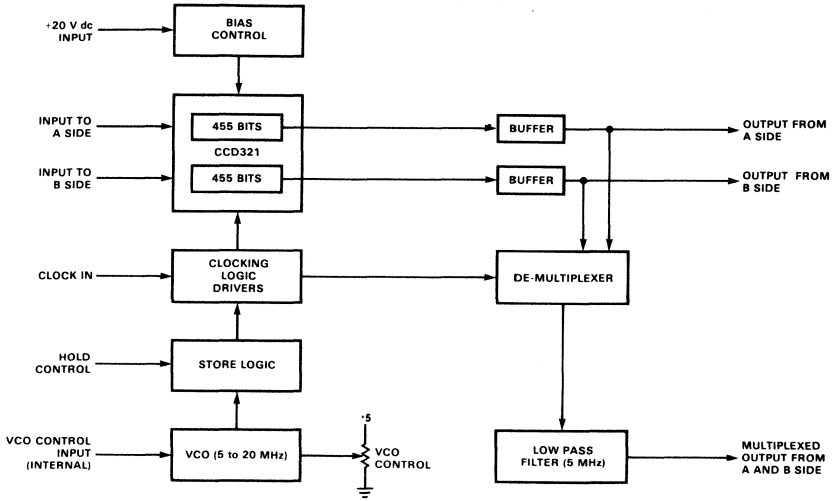
Typical video applications for the CCD321M include time-base correctors, video re-synchronising systems, comb filter realizations, moving target indicators and signal-to-noise enhancement systems. Other applications include time-base compression and expansion systems, phase delay equalizers and general purpose analog delay.

- **1 H DELAY LINE PERFORMANCE**
- **ELECTRICALLY VARIABLE DELAY**
- **ADJUSTABLE DELAY – BY CLOCK CONTROL**
- **WIDE SIGNAL BANDWIDTH – 5 MHz**
- **HIGH S/N RATIO – 55 dB**
- **DUAL 455-BIT OR SINGLE 910-BIT DELAY**
- **NO DRIFT – DELAY DEPENDENT ON CLOCK FREQUENCY**
- **INTERNAL OR EXTERNAL CLOCKING**
- **TEMPORARY STORAGE OPERATION CONTROLLED BY A SINGLE TTL INPUT LINE**
- **SINGLE POLARITY POWER SUPPLY – +20 V**



FAIRCHILD CHARGE COUPLED DEVICE • CCD321M

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Dual 455-Bit Analog Shift Register: CCD321

The Fairchild CCD321 is a monolithic 455/910-bit charge coupled device analog shift register packaged in a 16-pin dual in-line package. Functionally this device employs discrete electronic charge packets representing the sampled amplitudes of two analog input voltage waveforms that are transported towards output charge sensing amplifiers by a 1-1/2 phase digital clock signal. An integrated sample and hold output stage provides register output waveforms which are a near-replicas of the signals input to the device 455 periods earlier. (See CCD321 Data Sheet for more details concerning this device)

Clocking Logic and Driver Circuits

The transport and sampling clock pulses required for control of the CCD shift register are generated at TTL levels and then amplified and waveshaped by clock line drivers. A transport and a sample pulse for register A of the CCD321 is triggered by each LOW-to-HIGH transition of the master clock input to the CCD321M; a clock pair for register B is triggered by each LOW-to-HIGH clock input transition. Analog information is thus made to travel completely through both sides of the shift register by 455 complete cycles of the input clock.

Storage Logic

A TTL HIGH level on the Enable input terminal of the CCD321M is synchronized to the transport clock pulses and stops the transport and sampling functions of the register. The analog data in the registers when the clocks are stopped is stored until the Enable line returns LOW, and then transported out in the usual manner.

Signal Processing

Signal inputs to the A and B registers of the CCD321 are gain-controlled by individual potentiometers and then ac coupled through 22 μF capacitors into 100 K Ω loads at the device inputs. Two emitter-followers provide the sampled and held register A and register B output waveforms at a 75 Ω source impedance level.

If the two signal input terminals are connected together, the input data is sampled twice during each clock cycle. Alternate sampled analog bits go in sequence to the two registers of the CCD321. These alternating samples are de-multiplexed at the register output, low pass filtered, and given to a third video output lead. A 910-bit resolution is thus obtained, giving a signal delay of 455 clock periods or 910 clock half cycles. This multiplex operating mode provides 63.5 μs delay for a 5 MHz bandwidth signal using a clock input frequency of 2 x 3.58 MHz = 7.16 MHz, equivalent to a 14.3 MHz sampling and transport rate.

Clock Oscillator

The internal clock generator of the CCD321M is a VCO which can be controlled over a 5 to 20 MHz range by an external 0 to 5 Vdc signal, or adjusted by an on-board potentiometer. An external TTL compatible square wave clock signal can also be used by optional connector wiring.

Bias Control

Power input to the CCD321M is from a nominal +20 V external supply. On-board regulators control bias voltages for the CCD321, drivers, and logic circuitry.

FAIRCHILD CHARGE COUPLED DEVICE • CCD321M

DC CHARACTERISTICS

SYMBOL	PARAMETER	UNIT	CONDITIONS	MODULE PIN NUMBER
V_{CC}	Power Supply Input	+20 Vdc (< 400 mA)	Note 1	A & 1
V_{GG}	Common Ground	0 V	–	All unused pins
V_{IA}	Input to A side of CCD321	500 mV peak-to-peak	–	4
V_{IB}	Input to B side of CCD321	500 mV peak-to-peak	–	6
V_{OA}	Output of A side of CCD321	500 mV peak-to-peak	R_L = 1 kΩ	8
V_{OB}	Output of B side of CCD321	500 mV peak-to-peak	R_L = 1 kΩ	10
V_{OM}	Multiplexed Output	500 mV peak-to-peak 300 mV peak-to-peak	R_L = 1kΩ R_L = 75Ω	12
f_{IN}	Clock In	TTL Square Wave 0 – 25 MHz	Note 2	Z
f_{OUT}	Internal Clock	TTL Square Wave 5 – 20 MHz		22
τ	Input to Output Delay	$\frac{455}{f_{IN}}$	Single register or multiplex mode of operation	
		$\frac{910}{f_{IN}}$	Series mode of operation	
HOLD	Hold Control (Enable Input)	TTL Levels		20
VCO (IN)	VCO Control Input	0 – 5 Vdc		W
VCO(INT)	VCO Internal Control	0 – 5 Vdc		19

AC CHARACTERISTICS: T_A = 25°C, Multiplexed Mode of Operation, f_{IN} = 7.16 MHz V_{IA} = V_{IB} = 500 mV peak-to-peak, τ = 63.5 μs, See Note 3

SYMBOL	PARAMETER	VALUE	CONDITIONS
BW	Bandwidth (3 dB down)	5 MHz Min	
ΔG	Differential Gain	2.5%Max	Note 4
Δφ	Differential Phase	2.5° Max	Note 4
THD	Total Harmonic Distortion	2% Max	Note 5
S/N	Signal to Noise Ratio	55 dB Min	Note 6
T	Tilt of 60 Hz Square Wave	1% Max	
F	Band Pass Flatness: To 3.58 MHz	1 dB	
Offset	DC Offset in Temporary Storage Mode	2.5 mV/ms	Note 7

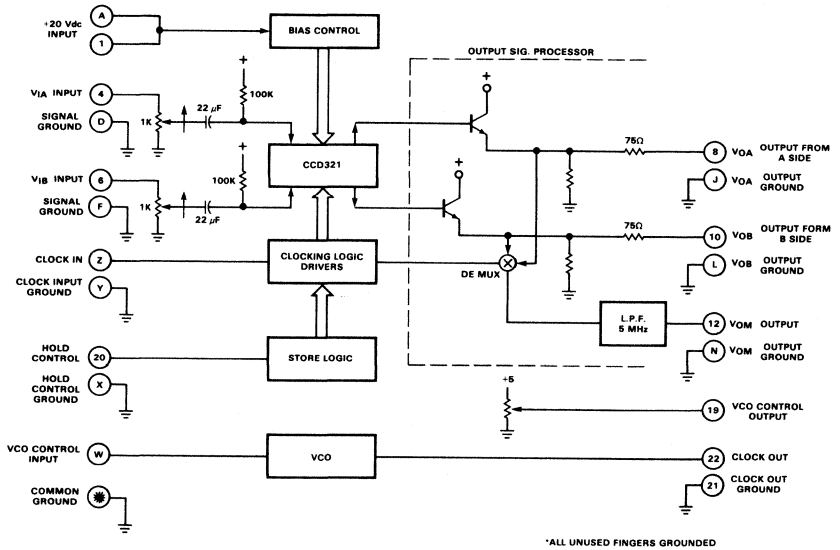
NOTES:
1. Module operates from 19 to 24 Vdc.
2. f_{IN} is the clock of a single register. In the series or independent register mode, a sampling clock of 4X the signal bandwidth is usually required. In the multiplex mode, a sampling clock of 2X the signal bandwidth is required. (i.e, in the multiplex mode of operation, with f_{IN} = 10 MHz per side a 5 MHz (3dB) bandwidth can be processed through the device.)
3. AC parameters guaranteed from 0°C to 55°C. Delay tolerances determined by stability of clock frequency.
4. Measured on a Tektronics 520 VECTORSCOPE.
5. Using f_{IN} = 10 MHz, multiplexed mode, V_{IA} = V_{IB} = 500 mV peak-to-peak, 1 MHz sine wave. Measurement done using spectrum analyzer.
6. Using Rhode and Schwartz noise meter at 4.2 MHz bandwidth.
7. This is a dc offset on the output signal which can occur because of dark current build-up when in hold mode. This offset can be expected to double for each 8-10°C increase in the CCD321 junction temperature.

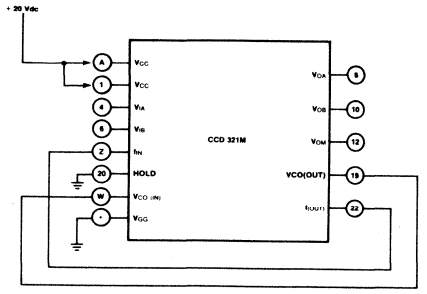
FAIRCHILD CHARGE COUPLED DEVICE • CCD321M

Modes of Operation and Connection Diagrams
The CCD321M can be operated in various modes: (1)Two independent 455-bit analog registers, (2) multiplex, (3) series and (4) temporary analog storage. An on-board generated clock with adjustable frequency, and internal VCO controlled clock or an independent externally generated clock input can be used in any of the four modes.

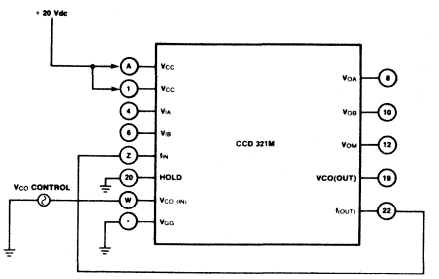
The circuit diagram shown below shows the pin nomenclature for the CCD321M.

The following diagrams represent the correct input/output connections for proper operation of the CCD321M in the various modes. The CCD321M circuit diagram is included in the module shipping package.

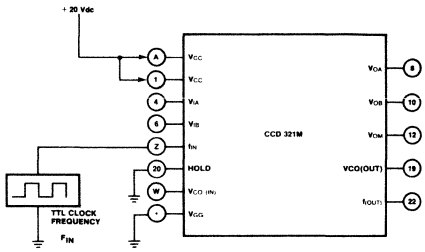




Mode 1: Internal Clock, Adjustable Frequency (R1)

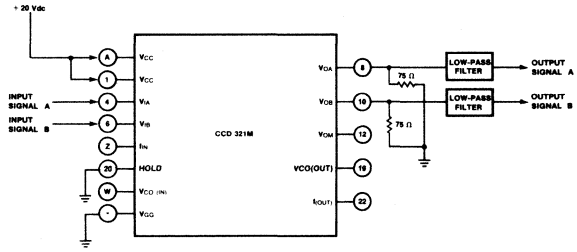


Mode 2: Internal Clock, V_{CO} Input Variable Delay



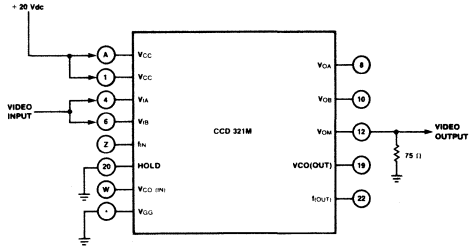
Mode 3: External Input Clock

Note 1: Delay = $\frac{455}{f_{IN}}$



Mode 4: Two Register Parallel Delay

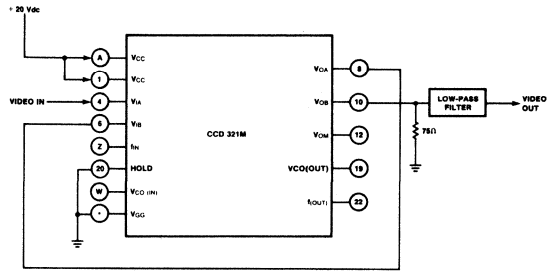
Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{455}{f_{IN}}$



Mode 5: Multiplexed Mode of Operation

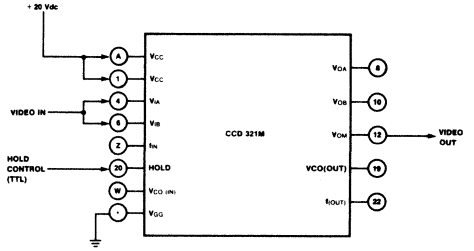
Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2, and 3.
2. Delay = $\frac{455}{f_{IN}}$

FAIRCHILD CHARGE COUPLED DEVICE • CCD321M



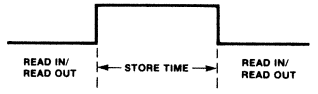
Mode 6: Series Mode of Operation

Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Delay = $\frac{910}{f_{IN}}$



Mode 7: Temporary Analog Storage Operation

Notes:
1. Depending on requirements, connect pins Z, W, 19 and 22 for internal or external clocking as shown in Modes 1, 2 and 3.
2. Store signal (TTL)



MECHANICAL SPECIFICATIONS
1. Module size is 4.5" X 5" X .75" (excluding edge connector).
2. Module weight is 5 oz.
3. Edge connector is 22-pin double readout, .156 center-to-center spacing. Mating connectors can be TRW type 50-44 series edge connector, or equivalent. Wiring information included with each module.

ORDER INFORMATION
To order a CCD321M, contact your nearest Fairchild sales office, representative or distributor. For any technical questions, contact Fairchild at 415-493-8001.

CCD323A*

DUAL 283-1/2 BIT CCD ANALOG DELAY LINE

PRELIMINARY DESCRIPTION

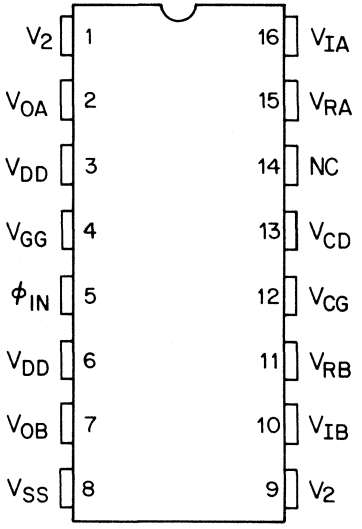
INTRODUCTION

The CCD323A is a dual 283-1/2 bits per channel, high speed video delay line. The input sampling frequency is controlled by an external clock input which is variable between 100KHz and 14MHz to result in delays between 2.835mS and 20.1μS. The device contains on-chip clock generator circuits so that only one external TTL level clock is required to operate the device. The dc voltages that are necessary to bias the device are very much like those used for biasing CCD321A. With 238-1/2 bits length and clocking done at ≃4.4MHz, the device produces a delay of ≃64μS to ideally suit PAL TV Applications.

*The device described in this preliminary specification is currently available in sample quantities only. We are investigating potential market for this part and welcome customer inputs as to its application. At this time the part should not be designed into your volume application without first contacting the factory regarding future availability. (415) 493-8001

Ordering code CD323ADC*

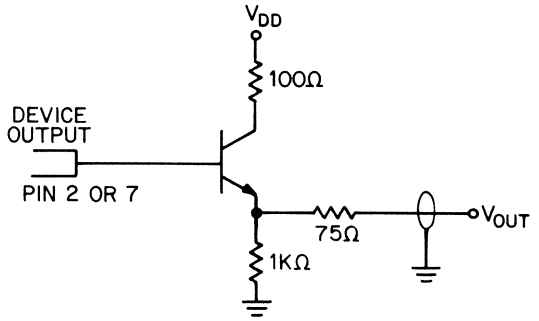
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)



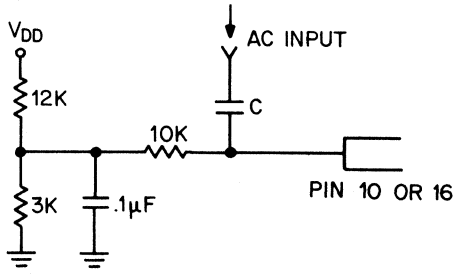
PIN NAMES AND DEFINITIONS

V_2	Analog Shift Register DC Transport Phase	DC voltage ≈1/2 of internal clock amplitude or about 6V.
V_{OA},V_{OB}	Analog Outputs	Outputs of channels A, B. (See Note 1)
V_{DD}	Output Drain	Amplifier supply voltage of +15V.
V_{GG}	Signal Ground	0.0V
$\emptyset_{IN}$	Clock Input	TTL level clock input. CCD clocks are generated on-chip using this waveform.
V_{SS}	Substrate Ground	0.0V
V_{IA},V_{IB}	Analog Inputs	Constant DC bias mode. The input AC signal to be delayed is applied to this pin via an AC-coupled network. (See Note 2)
V_{RA},V_{RB}	Analog Reference	DC voltage varying from +4V to +6V. This is the input reference bias for the CCD and in conjunction with V_{IA} and V_{IB}, establishes the operating conditions of the CCD.
V_{CG}	Clock Circuit Ground	0.0V
V_{CD}	Clock Driver Drain	Clock driver supply voltage of +15V.
NC	No Connection	Do not ground

NOTE 1: OUTPUT SCHEME



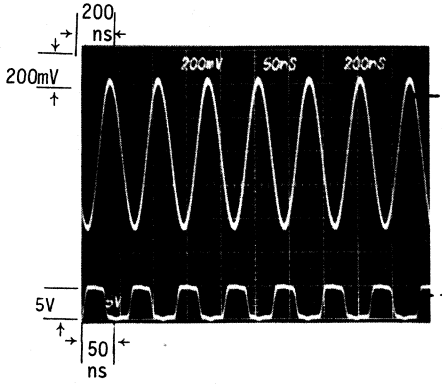
NOTE 2: INPUT SCHEME



TESTING PROCEDURE

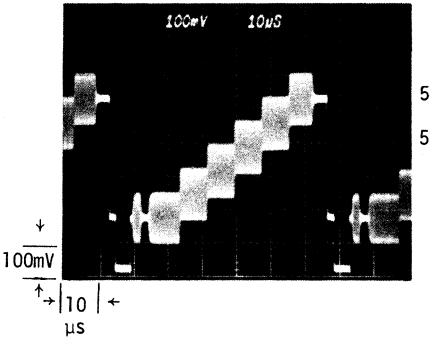
Arrange the DC voltages as above and apply a TTL level clock of 2MHz to $\emptyset_{IN}$ to clock the device. An input sine-wave signal of 500KHz and amplitude 500mV pp is applied to the AC input (A or B, or both). Vary V_{RA} (and/or B) to get the delayed output signal. A filter with 3dB cutoff at the upper signal frequency is recommended after the emitter follower in the output of the device. This reduces the clock coupling in the output. Once the device is operating, $V_{RA/B}$, the input AC signal amplitude/frequency and clock frequency may be altered to suit your application.

TYPICAL OUTPUT CHARACTERISTICS



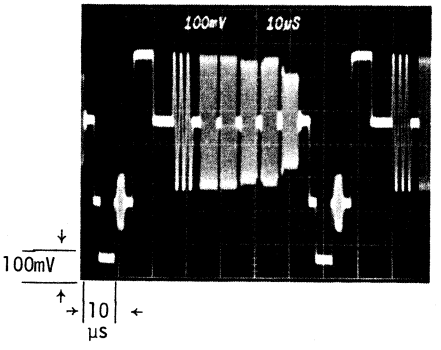
AC Output (filtered)

TTL Level Clock Input



5 - Step Linearity Test

5 - Step Output with 3.58MHz Color Burst



Response to NTSC Color Burst

ELECTRICAL PERFORMANCE CHARACTERISTICS (TYPICAL) - FOR BOTH CHANNELS

BANDWIDTH: Better than 4.5MHz at 14MHz clock

S/N RATIO: Better than 58 dB

DIFFERENTIAL GAIN: $\leq$ 3%

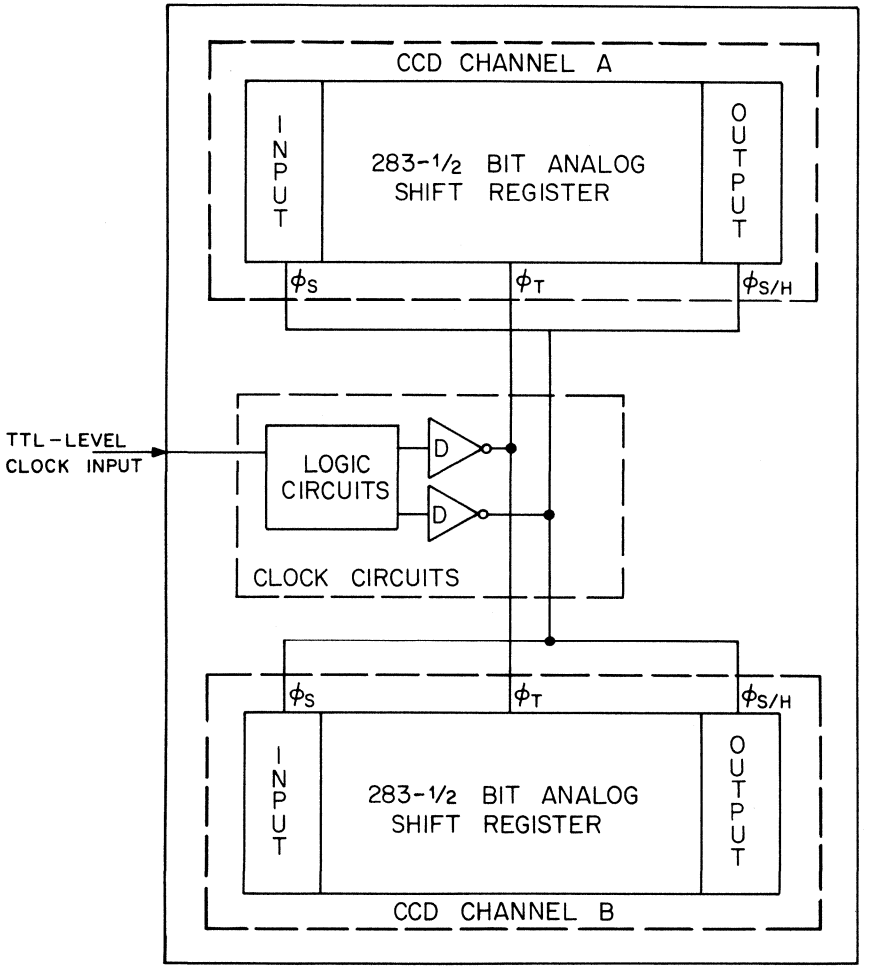
DIFFERENTIAL PHASE: $\leq$ 3 degrees

CLOCK RATE: MIN: 100KHz MAX: 14MHz

OUTPUT DC LEVEL: $\simeq$ +9.0V

NOTE: THE ABOVE VALUES ARE MEASURED AT A 700mV PEAK-TO-PEAK VIDEO OUTPUT.

BLOCK DIAGRAM



ϕ_S – INPUT SAMPLING CLOCK
ϕ_T – CHARGE TRANSPORT CLOCK
$\phi_{S/H}$ – OUTPUT SAMPLE AND HOLD CLOCK
D – DRIVER

FAIRCHILD
A Schlumberger Company

CCD

Cameras

CCD IMAGING AND SIGNAL PROCESSING

IMAGING

Camera Subsystems

Fairchild CCD Camera subsystems are fully assembled and calibrated electro-optical instruments useful in a wide variety of scientific and industrial applications.

Fairchild CCD camera subsystems are ideally suited for computer interfaced system use. Their I/O compatibilities allow operation in response to computer generated signals or asynchronously while providing computer output signals.

The precise geometric accuracy of CCD image sensors make computer processing of optically acquired data practical for many image processing or data analysis applications.

Each camera subsystem includes a camera head which can be supplied with a variety of standard "C" mount lenses, a control unit and associated interconnecting cables.

Camera accessories are available to adapt the basic subsystem to customer requirements.

Line Scan Camera Subsystems

The Fairchild line scan camera subsystems are versatile electronic instruments useful in non-contact optical measurement and data acquisition applications. At the heart of the systems are charge coupled device line scan image sensors providing resolutions of 256, 512, 1024, 1728 or 2048 elements per scanned line. The cameras are used for a wide variety of applications in industrial process controls such as position and size measurements, defect and surface flaw detection as well as general purpose optical recognition of object shapes and sizes.

- Optical resolution up to 2048 elements per scanned line.
- Precise geometric accuracy.
- High-speed data rate up to 10 MHz.
- Exposure time, line scan rate, and video data rate adjustable over wide ranges.
- High sensitivity of CCD sensor permits low light level operation.
- Dynamic range of greater than 200 to 1.
- Solid-state ruggedness and reliability.
- Sample-and-hold video output signal provided.

Applications

The Line Scan camera subsystems find applications in the general areas of non-contact industrial optical inspection and optical data acquisition. The Line Scan Camera subsystems are particularly applicable for use with objects that are generally in motion, i.e., carried by a conveyor mechanism. The precise metric accuracy and digital scanning capability of these subsystems allows easy development of highly sophisticated systems for process and quality control of manufacturing processes.

- Position measurement.
- Size and shape measurement.
- Defect and surface flow detection and categorization.
- Object sorting for size, shape, color or other optically-measureable attributes.
- Gray level detection capability for density measurements.
- General purpose inspection applications.
- BAR code readers for material handling systems.
- Facsimile, OCR, microfiche, and mark-sensing data acquisition.

Specifications

Characteristic	CCD1100C	CCD1200C	CCD1300C	CCD1400C	CCD1500C
Sensor	256x1	512x1	1024x1	1728x1	2048x1
Line Scan Rate	60Hz-35kHz	60Hz-20kHz	60Hz-10kHz	60Hz-6kHz	60Hz-5kHz
Exposure Time	30μs-16ms	51μs-16ms	102μs-16ms	175μs-16ms	204μs-16ms

Data Rate: 100kHz-10MHz, Dynamic Range: ≥200:1, Responsivity: 16V/ft cds

The CCD1400 Line Scan Camera is being discontinued. Stock is currently available in small quantities only.

CCD LINE-SCAN CAMERAS MODELS CCD1100, 1300 AND 1400

INCLUDING LENS, CAMERA, CONTROL UNIT, AND INTERCONNECTING CABLE

FEATURES

EASE OF OPERATION

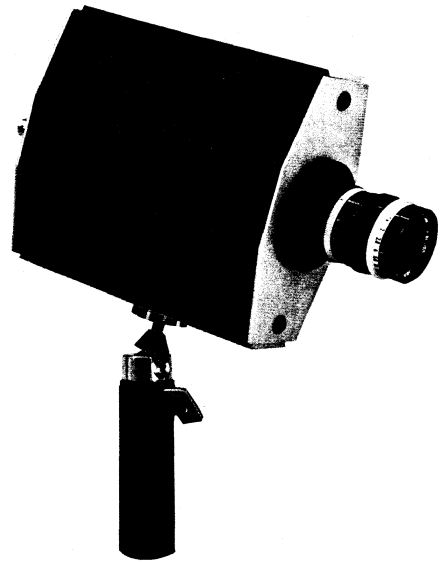
SOLID STATE RELIABILITY

COMPUTER COMPATIBLE
- 0-1 V sample-&-hold video
- Binary video
- Video valid indication
- Internal or external clock control
- Variable exposure time
- Power line synchronized exposure control
- Automatic or fixed gain control

OPTICAL FLEXIBILITY
- Interchangeable C-mount lenses
- Operational without a lens for some applications
- Visible light response
- AGC provides contrast control
- Resolution - 256, 1024 or 1728 elements

MECHANICAL
- Compact
- Tripod, dovetail, faceplate mountable
- Lightweight

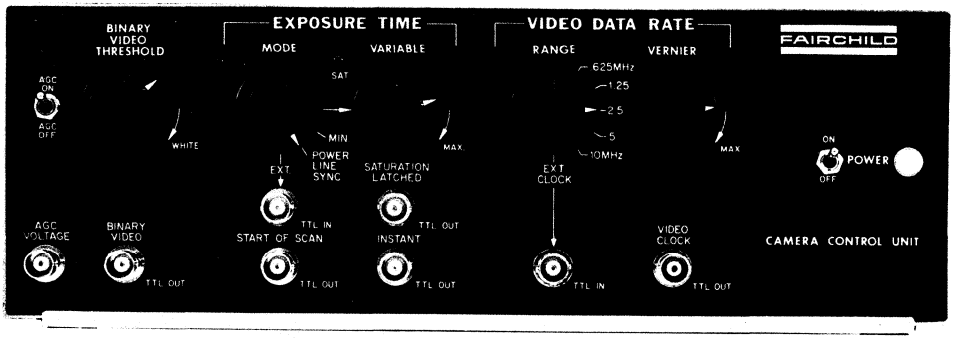
ADVANTAGES OF CCD TECHNOLOGY
- High sensitivity
- Precise photosite spacing
- Low internal operating voltages.



GENERAL DESCRIPTION - The CCD Line Scan Camera is a versatile electronic camera that is easy to operate. A line scan array in the camera senses a line of optical information and produces an analog waveform proportional to the brightness of the image. When motion is applied to the object being sensed, a complete picture or series of line-scan outputs is generated. The system can be used for precision non-contact measurements, facsimile sensing, velocity measurements, surface flaw detection, shape recognition sorting and many other optical sensing functions.

FUNCTIONAL DESCRIPTION - Model CCD1100, CCD1300 and CCD1400 are complete Line-Scan Cameras consisting of a CCD Line-Scan Camera, Control Unit, and interconnecting cable. The subsystem provides all of the necessary control and signal processing functions for realization of a flexible high performance line-scanning camera system. The subsystem permits precise measurement and sensing of optical data. Applications requirements such as document scanning, industrial inspection, surveillance, spectroscopy, microscopy and precision measurements can be satisfied with the subsystem.

LINE SCAN CAMERA - The Line-Scan Camera contains a CCD linear sensor of 256, 1024 or 1728 elements of resolution, a timing control module, a signal processing module and a rugged housing that may be tripod, front faceplate, or dovetail mounted. Selection of a standard lens compatible with the application completes the optical sensing system. A camera to control unit interconnection cable permits complete remote control of the camera by the Control Unit. The Control Unit also accepts input to permit camera control by a microprocessor or computer.



CAMERA CONTROL UNIT - The Camera control Unit, provides four principal operating functions; video output control, video data rate control, exposure control and the camera power supply.

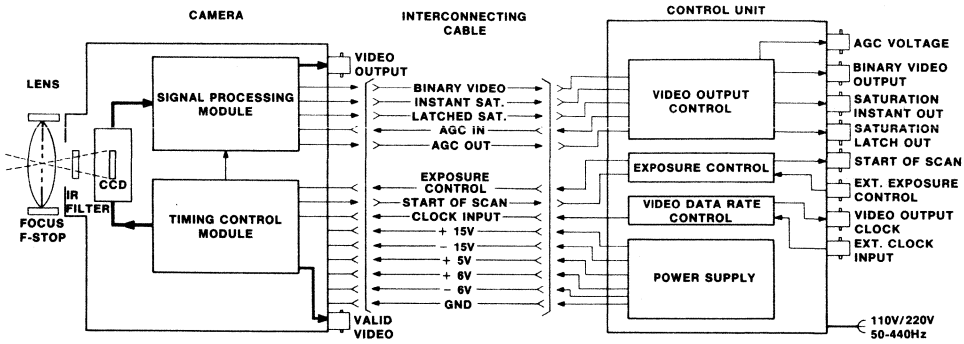
VIDEO OUTPUT CONTROL - A switch selection for automatic gain control or fixed gain is located on the front faceplate. The AGC operating mode is useful for signal compensation due to aging of light source or variations in paper color when scanning facsimile documents. An AGC voltage terminal (BNC) is available for further signal processing. A binary-video threshold adjustment potentiometer controls digital quantizing of the output signal over the complete signal range. A TTL level binary-video output signal is available on the front panel BNC connector.

VIDEO DATA RATE - A video clock oscillator is located in the video data rate section. A 6-position switch and a Vernier potentiometer are also included to permit continuous frequency adjustment from 10 MHz to 100 kHz. An input for externally generated clock pulses can be utilized to synchronize camera operation with an external system.

EXPOSURE CONTROL - The exposure control can operate in two modes: synchronously (under the control of a computer or the control unit), and asynchronously (under the control of the camera). System flexibility is enhanced by these two modes. Another particularly useful feature of the exposure control permits the sensing subsystem to be synchronized with the power line. When utilizing a fluorescent or other ac powered illumination source, no amplitude modulation by the light source appears on the output signal. When the exposure control switch is located in the position marked "variable", an infinite selection of exposure time can be selected. The minimum exposure time is set by the video line rate and the maximum can be adjusted to 16 ms. BNC connectors are available for all incoming and outgoing signals. A light-emitting diode, when on, indicates that the device has saturated. A saturated condition causes no permanent degradation to the sensor or the subsystem.

CAMERA POWER SUPPLY - The control unit can be powered by either a 110 V ac or 220 V ac, 50-440 Hz power line. Switch selection of this option is located on the rear of the unit. A power supply internal to the control unit provides ± 15 V and + 5 V to the camera through the interconnecting cable.

SUBSYSTEM BLOCK DIAGRAM



SPECIFICATIONS - Model 1100, 1300 and 1400
Line Scan Camera Subsystem

PERFORMANCE

Sensor	Model CCD1100: 256×1 CCD110F Model CCD1300: 1024×1 CCD131 Model CCD1400: 1728×1 CCD121H
Geometric Distortion	System performance is determined by lens selected.
Dynamic Range	≥200:1
Responsivity	16 V/ft cd s using a 2854 °K, tungsten source
Photoresponse Non-Uniformity	± 50 mV measured at 500 mV output level using fixed gain setting
Saturation Exposure	0.06 ft cd s

VIDEO OUTPUT

Analog	$1V_{pp}$ video (75Ω)
Binary	"1" = White, "0" = Black
AGC Range	20 db
Data Rate	100 kHz to 10 MHz
Line Scan Rate	60 Hz to 35 kHz for CCD1100, 60 Hz to 10 kHz for CCD1300, 60 Hz to 6 kHz for CCD1400
Exposure Time	30 μs to 16 ms for CCD1100, 102 μs to 16 ms for CCD1300, 175 μs to 16 ms for CCD1400
SPECTRAL RESPONSE	Approximately visible response
INPUT POWER	105 - 125 V_{ac} 50-440 Hz 0.1 A 210 - 240 V_{ac} 50-440 Hz 0.05 A

POWER REQUIREMENTS

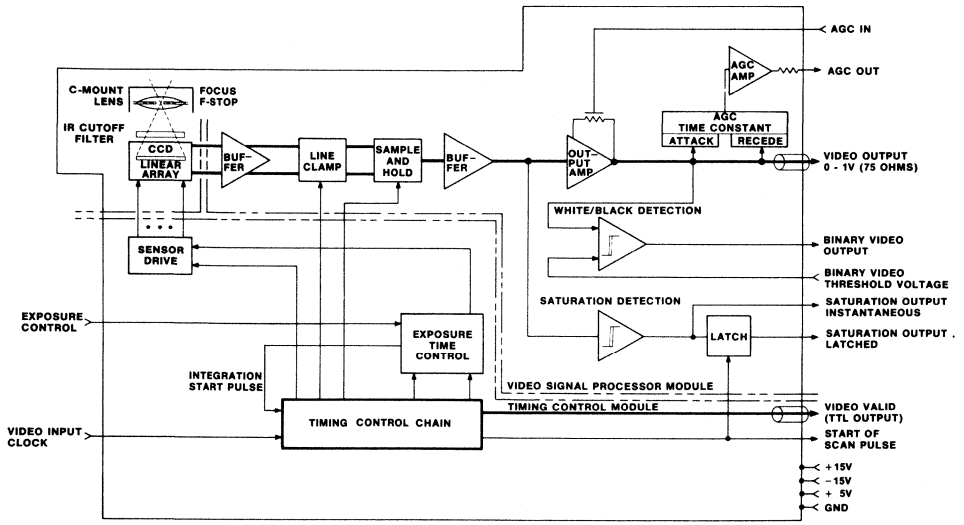
Camera	Control Unit
+15 V 150 mA	+15 V 50 mA
−15 V 100 mA	−15 V 60 mA
+ 5 V 350 mA	+ 5 V 100 mA
+ 6 V 50 mA	
− 6 V 60 mA	

TEMPERATURE	0 °C to 40 °C

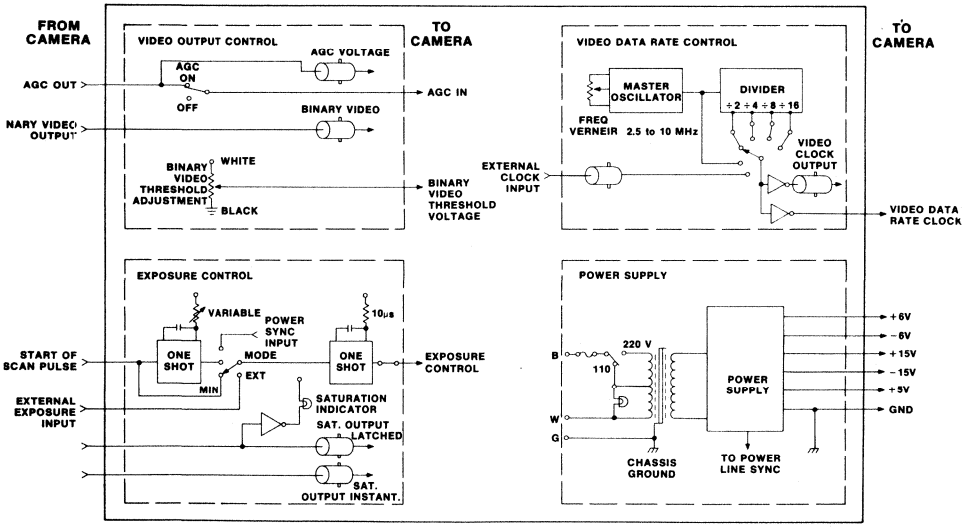
PHYSICAL DATA

	Camera	Control Unit
Size (without lens)		
Width	2.6" (6.6 cm)	12.0" (30.5 cm)
Height	5.5" (14.0 cm)	4.1" (10.4 cm)
	6.0" (15.2 cm)	8.0" (20.3 cm)
Weight	1.7 lbs (0.77 kg)	5.4 lbs (2.45 kg)
Connector	CINCH DB-255 F179 BNC's	CINCH DBC-255 BNC's
Mount	Tripod 1/4 x 20 Dovetail Front Faceplate	

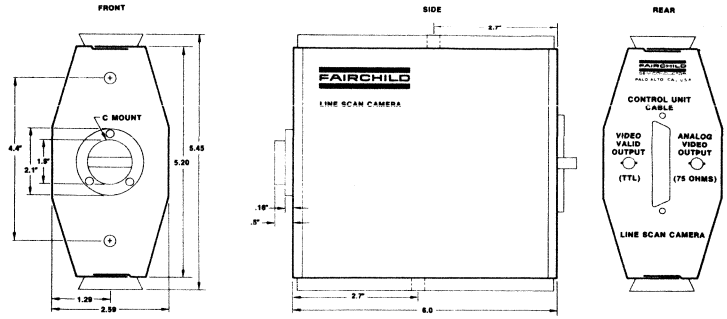
LINE SCAN CAMERA BLOCK DIAGRAM



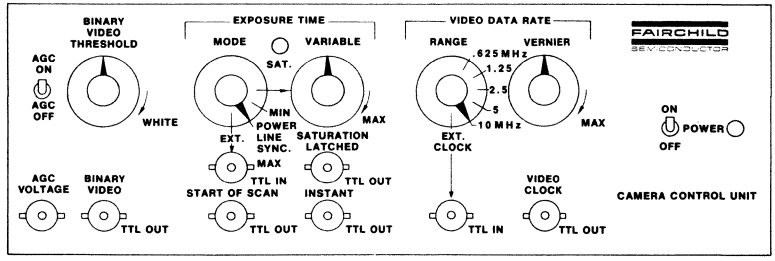
CONTROL UNIT BLOCK DIAGRAM



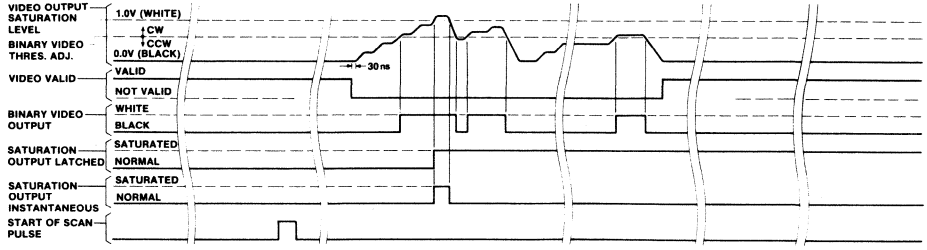
PHYSICAL CONFIGURATION OF LINE SCAN CAMERA



PHYSICAL CONFIGURATION OF CONTROL UNIT



TIMING DIAGRAM
LINE SCAN CAMERA SUBSYSTEM



NOTE: EACH VIDEO CLOCK PULSE CORRESPONDS TO A SINGLE PICTURE ELEMENT (PIXEL)

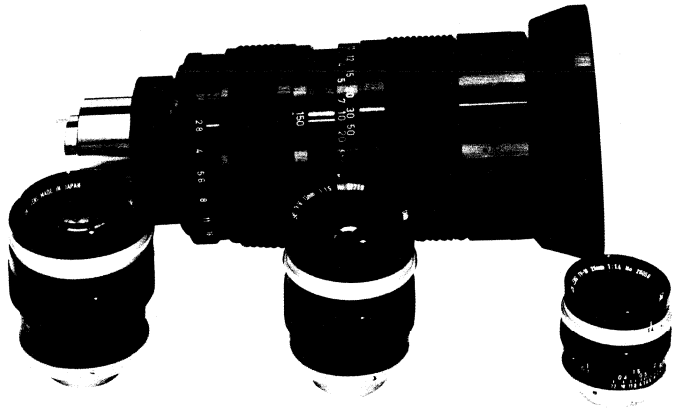
SIGNALS — TO AND FROM THE CAMERA UNIT

ANALOG SIGNALS

SYMBOL	CHARACTERISTICS	RANGE MIN	RANGE TYP	RANGE MAX	UNITS	DEFINITIONS
OUTPUT — Analog Video Signals						
VO	Video Output					2
	Black		0		V	
	White		1.0		V	
	Dynamic Range		≥200:1			13
	Acquisition Time		30		ns	14
	Slew Rate		20		V/μs	15
	Random & Coherent Noise		5		mV p-p	16
AGCO	Automatic Gain Control Output				mV p-p	9
	Gain Range	9:1	10:1	11:1		
	Max Gain (10:1)		0.6		V	
	Min Gain (1:1)		−4		V	
INPUT - Analog Video Signals						
AGCI	Automatic Gain Control Input					10
	Max Gain (10:1)		0.6		V	
	Min Gain (1:1)		−4		V	

DIGITAL SIGNALS

OUTPUT - Digital Video Signals TTL Levels						
BVO	Binary Video Output					1
	"1" = White	≥2.4			V	
	"0" = Black			≤0.8	V	
SOL	Saturation Output Latched					12
	"1" = Saturation	≥2.4			V	
	"0" = Normal			≤0.8	V	
SOI	Saturation Output Instantaneous					11
	"1" = Saturation	≥2.4			V	
	"0" = Normal			≤0.8	V	
VV	Video Valid					4
	"1" = Not Valid	≥2.4			V	
	"0" = Valid			≤0.8	V	
SOS	Start of Scan					5
	"1" = Start	≥2.4			V	
	"0" = Hold			≤0.8	V	
INPUT - Control Signals - TTL Levels						
EC	Exposure Control					8
	"1"	≥2.4			V	
	"0"			≤0.8	V	
VIC	Video Input Clock					7
	Frequency	0.1		10.0	MHz	
	Voltage	≥0.8		≥2.4	V	



LENSES FOR CCD LINE SCAN CAMERA

Lens Focal Length	Maximum Relative Aperture	Angular Field of View CCD1100	CCD1300	CCD1400	Lens Mount
13 mm	F = 1:1.8	16°	60°	91°	C
25 mm	F = 1:1.5	8.5°	33°	54°	C
50 mm	F = 1:1.4	4.2°	17°	28°	C
75 mm	F = 1:3.2	2.8°	11°	19°	C
ZOOM 15 to 150 mm	F = 1:2	14 to 1.4°	53° to 5.6°	82° to 9.5°	C

PARAMETER FOR LENSES OF LINE SCAN CAMERA

OPTICAL CONSIDERATIONS

IMAGE DETECTOR SYSTEM

The image detector utilized by the Line Scan Camera is a monolithic silicon charge-coupled-device structure, which is packaged in a hermetically sealed DIP equipped with an optical-quality glass window.

Sensor Operation

Photo detection in the CCD structure is accomplished in a single row of image sensor elements which are separated by diffused channel stop barriers. The detection mechanism is accumulation of free electrons generated by the photon absorption process. The charge built up in individual photosites is a linear product of the incident illumination intensity and the exposure time over which the electrons are allowed to accumulate.

The charge accumulated within each of the individual photosites is transported sequentially out of the CCD image sensor during a VIDEO VALID scanning line readout period. After further processing, including a sample and hold function, the accumulated charge data becomes the camera's ANALOG VIDEO OUTPUT signal. This signal has an instantaneous amplitude representing the spatial distribution of image brightness along the row of photo detection sites as a function of time. The readout DATA RATE is the subsystem VIDEO CLOCK frequency.

Image detection is a true time integration function: charge is accumulating in each photosite during the total EXPOSURE TIME period which extends from the beginning of one scanning line readout interval until 28 video clock periods preceding the next readout interval. Satisfactory exposures can be made with short flashes from strobe lights or constant-intensity images, depending upon the subject. (Unlike photographic film, the CCD sensor does not suffer any reciprocity failure with very short illumination durations.)

Sensor Geometry

The photo-sensitive area of the image sensor is a row of 256, 1024 or 1728 elements which are on 13 micrometer (0.51 milli-inch) center-to-center spacing. Each sensing site is 13 μ x 13 μ for the CCD1300 and 13 μ x 17 μ for the CCD1100 and CCD1400. The length of the entire photo-sensitive row is 3.3 mm for the CCD1100, 13.3 mm for the CCD1300, and 22.5 mm for the CCD1400. In terms of spatial frequency, the resolution of the image sensor (and therefore of the camera) is 38.4 line pairs per millimeter (lp/mm).

Spectral Response

The spectral response of the Camera has been shaped to a rough approximation of human photopic sensitivity by inclusion of an optical filter glass in the lens holder to decrease infrared sensitivity. This has been shown to give good results in most applications. The filter can be removed, at the purchaser's option, but will result in lower resolution because long-wavelength photons are absorbed deep in the silicon bulk, which leads to inter-element crosstalk.

LENS SELECTION

From a practical viewpoint, selection of a lens for the Line Scan Camera Subsystem is similar to selection of a lens for a photographic camera. Due consideration must be given to the object-to-camera separation, required resolution in the object plane, required depth of focus, available light power density, object size, etc.

Magnification

As used here, "magnification", (M), is defined as the ratio of the object length to the length of the image of the object upon the array. M can be easily derived from the familiar lens equation:

$$\frac{1}{F} = \frac{1}{ID} + \frac{1}{OD}$$

$$M = \frac{OD}{ID} = \frac{OL}{IL}$$

where F = lens focal length, OD = lens-to-object distance (= working distance), ID = lens-to-sensor surface distance at focus, OL = length of object, IL = length of object image upon sensor surface.

Required Illumination

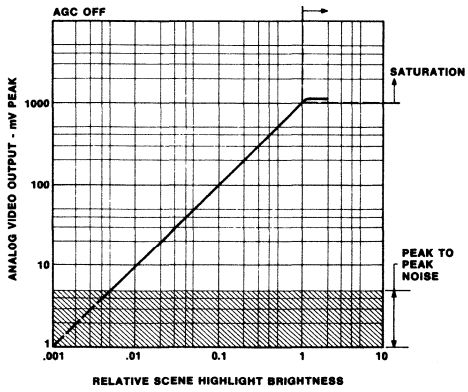
Illumination requirements vary radically, depending upon the camera application. Good results can many times be obtained by use of a power-line driven fluorescent illuminator, and operating the camera in the LINE SYNC exposure control mode. Shorter exposure times will require higher intensity illumination of the object. Either backlighting or frontlighting systems can be used. One way to determine the illumination requirements is to consider the CCD sensor as equivalent to a photographic film with an ASA speed of about 100, and to calculate F-stop and exposure time accordingly.

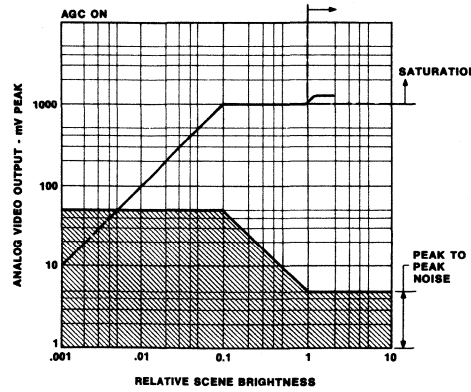
For special help with illumination, such as special filters or light sources, consult the factory at (415) 493-7250.

DEFINITIONS

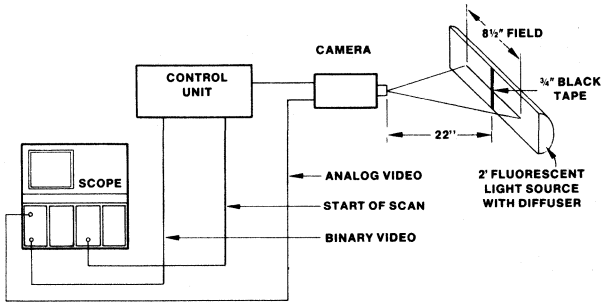
1. Pixel - Picture element. There are 256, 1024 or 1728 pixels in each scanned-line output.
2. Analog Video Output - A sample and hold output waveform whose amplitude is proportional to the light which each picture element has received during the preceding exposure time.
3. Binary Video Output - A digitized representation of the analog video output; "0" represents black, "1" represents white. The analog video is processed by an analog comparator. An adjustable reference level permits "1"/"0" decision at any voltage level between 0 and 1 V.
4. Video Valid Output - A TTL signal that is LOW ≤(0.8 V) only during the video clock intervals when actual video data output is available.
5. Start of Scan Output - A TTL signal that can serve as a sync pulse; it goes HIGH for one video clock period immediately preceding the video valid output interval.
6. Video Clock Output - A TTL output signal that indicates the rate at which photosensor element charge packets are being delivered to the output.
7. Video Input Clock - The video output rate of the camera can be controlled by an external clock-generator signal to the external clock input of the control unit.
8. Exposure Time - The amount of time the image sensing elements are allotted to view the image. Control of the exposure time can be synchronized to the camera, synchronized to the control unit (computer or other external source) or synchronized to the power line.
9. AGC Output - An analog signal that represents the magnitude of the gain necessary to amplify the highest pixel to 1 V output.
10. AGC Input - An analog signal that controls the gain of the output amplifier. A gain range of 1X to 10X input signal can be accomplished.
11. Saturation Output Instantaneous - The presence of a "1" level indicates that the respective pixels have exceeded the highest possible level permitted for good signal fidelity.
12. Saturation Output Latched - A TTL indication that indicates the occurrence of a saturation condition during one line of video information. An LED is illuminated upon saturation.
13. Dynamic Range - The analog video output signal level resulting from saturation exposure divided by the peak-to-peak noise content of one video output pixel.
14. Acquisition Time - The time required for the sample and hold circuitry to acquire the associated voltage of next charge packet.
15. Slew Rate - The speed at which the output amplifier can change from the value of one pixel to the value of the next pixel. At a 10 MHz video rate, a full scale output change from one pixel to the next pixel can be accomplished.
16. Random and Coherent Noise - The peak-to-peak noise that appears at the analog video output (excluding dark singal) when no illumination derived signal is present.

SUBSYSTEM CHARACTERISTICS

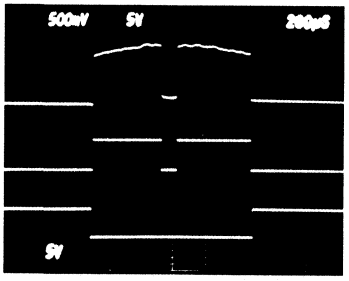




SIMPLE SYSTEM BLOCK DIAGRAM USING CCD1300 SYSTEM



THE FOLLOWING WAVEFORMS WERE TAKEN FROM AN OSCILLOSCOPE WHILE THE CAMERA WAS VIEWING A FLUORESCENT LIGHT FIXTURE WITH A 0.75 INCH BLACK TAPE IN THE MIDDLE.

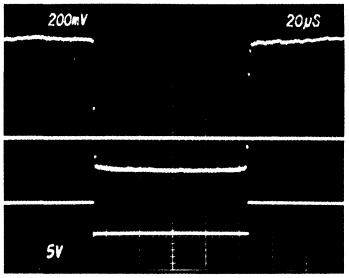


VIDEO OUTPUT

BINARY VIDEO OUTPUT

VIDEO VALID

1 = WHITE
0 = BLACK
1 = NOT VALID
0 = VALID

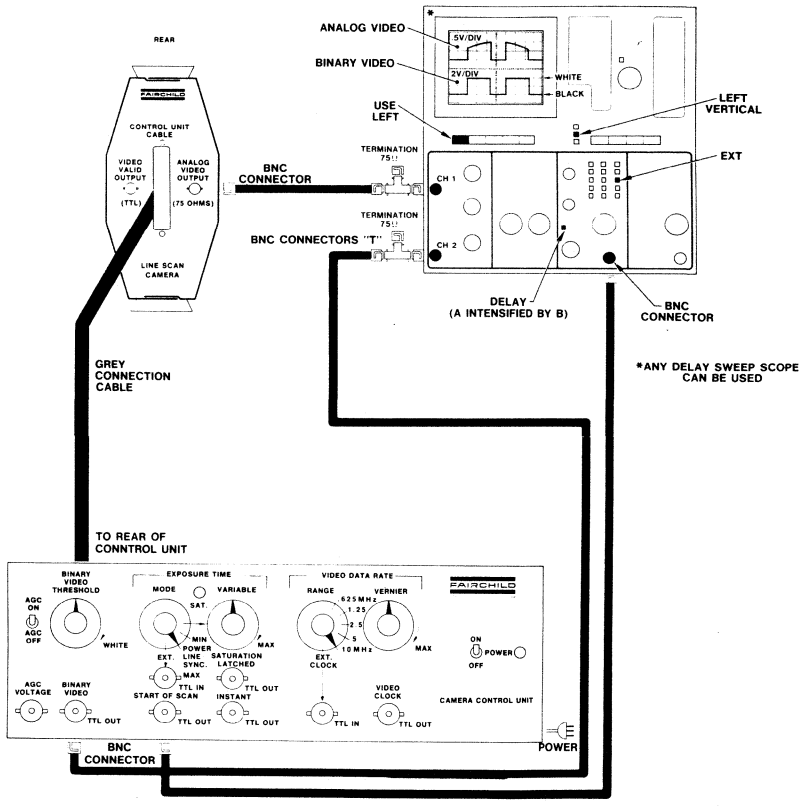


VIDEO OUTPUT EXPANDED

BINARY VIDEO THRESHOLD

BINARY VIDEO

BASIC CONNECTION DIAGRAM



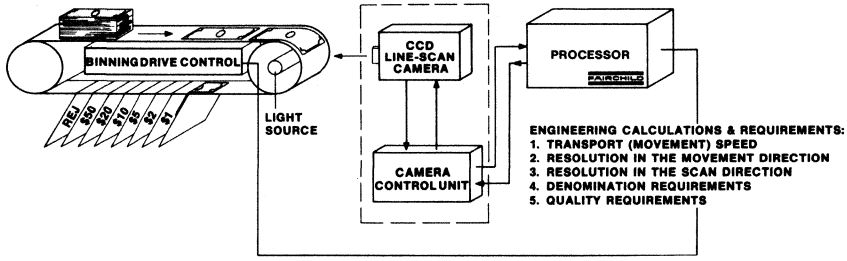
APPLICATION: SCANNING/RECOGNITION SYSTEM

SYSTEM DESCRIPTION

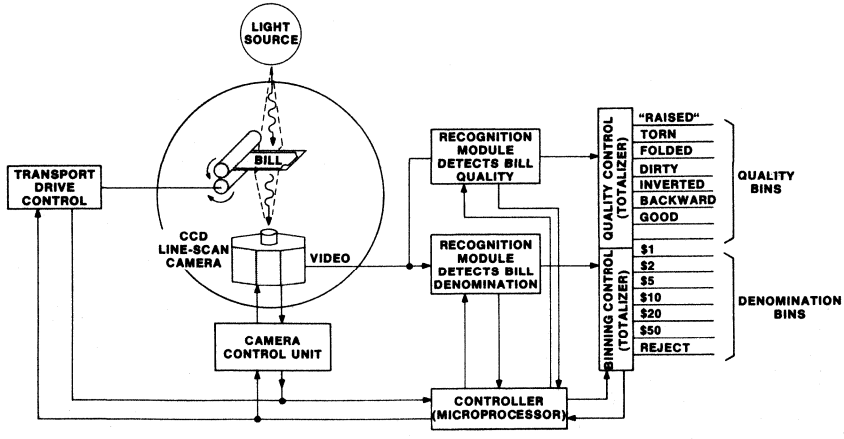
The Line-Scan Camera subsystem is a powerful scanning and/or recognition tool when combined with a computer or microprocessor. The technique used here, shows a rear lighted document being sensed by the line scan camera. A digital representation (ROM) of the desired object is stored in the microprocessor memory and is placed in synchronization with the unknown object located on the transport. When both the camera output and the microprocessor output indicates that a match has been established, the proper binning control is activated to receive the document. If insufficient criteria is available for determination of a match, the binning selection controller places the bill in the rejection bin. When properly programmed, documentation quality as well as value or denomination can be determined.

This technique is adaptable to automatic sorting systems, where only a few (or many) defects must be found in a large population. By implementing object viewing masks in the microprocessor, only certain fields of optical information in the object can be selected for processing. All other areas of the object are ignored.

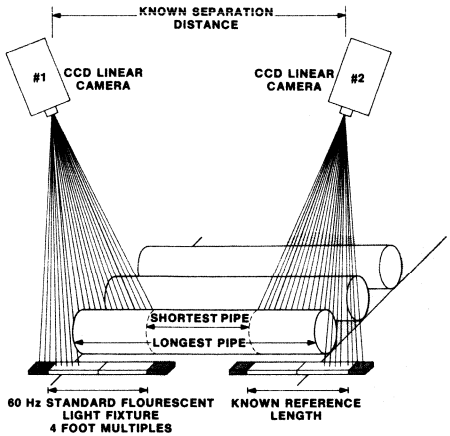
PICTORIAL VIEW
SCANNING AND RECOGNITION SYSTEM



BLOCK DIAGRAM
SCANNING AND RECOGNITION SYSTEM



PICTORIAL VIEW
MEASUREMENT SYSTEM



APPLICATION: MEASUREMENT SYSTEM

FEATURES:

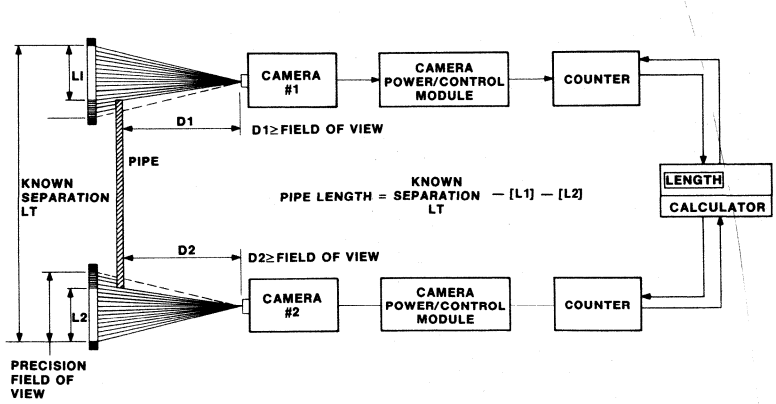
- Standard fluorescent light fixture
- Easy to align and maintain
- Self calibrating feature for
  - length
  - light level (AGC)
- Accurate Calculator permits taking many samples and averaging.

SYSTEM DESCRIPTION

By positioning two CCD Line Scan Cameras outside of the longest object and knowing the separation of the reference end points, length can be determined. The technique utilized here, senses the bottom edge of the object (closest to the floor) to eliminate effects of varying diameters or thicknesses. A standard 60 Hz fluorescent light source facing toward the camera can be used as the illumination source; a good black/white transition is necessary. The output of each camera is fed into a counter with bcd output. Since, the distance (LT) is known, the distance from each edge to the transition is determined by the camera. Subtracting L1 + L2 from LT produces the length of the pipe when corrections for lens magnification are made by the programmable calculator. These corrections can be implemented by a lookup table or an equation within the calculator.

This technique is adaptable to area and volume measurements as well as length. Gap, thickness, and position measurement and/or correction systems can be implemented when the camera is used as a feedback sensor to a controller.

BLOCK DIAGRAM



FAIRCHILD
A Schlumberger Company

Fairchild Camera and Instrument Corporation
CCD Imaging

CCD1200/1500 COMMERCIAL LINE SCAN CAMERAS

Supplement to CCD1100/1300/1400 Data Sheet

The CCD1200 and CCD1500 cameras, although not contained in this data sheet, are functionally described by it. The differences are in the sensors employed. The CCD1200 camera utilizes a 512x1 sensor, which has elements positioned on 13µm centers. Each photosite is 13µmx13µm. The CCD1500 camera employs the CCD143 sensor, a 2048x1 element array. Its 13µmx13µm photosites are also positioned on 13µm centers. Since the maximum data rate of the camera is 10MHz, maximum line rates and minimum exposure times are fixed by the number of elements in the sensor. For the CCD1200 camera, line scan rates can be adjusted over the range of 60Hz to 20KHz and exposure time can be adjusted from 51µS to 16mS. For the CCD1500 camera, the ranges are 60Hz to 5KHz and 204µS to 16mS, respectively.

The CCD1100, 1200, 1300, and 1400 make use of a standard 'C' mount for lens attachment. The CCD1500 uses a bayonet lens mount to achieve the wider field of view necessary for the longer CCD143 array.

The CCD1100 and CCD1300 now employ the CCD111 and CCD133 sensors, respectively replacing their functional equivalents, the CCD110F and CCD131.

Note also, that the ordering codes for the cameras and camera accessories in the back of the sheet are obsolete. Please refer to the CCD Imaging Price Sheets for the correct ordering codes.

PIXEL LOCATOR

FOR THE

CCD1100, CCD1300 and CCD1400
FAIRCHILD LINE SCAN CCD CAMERAS

OPTION MODEL NUMBERS

CCD1120-02
CCD1320-02
CCD1420-02

GENERAL DESCRIPTION

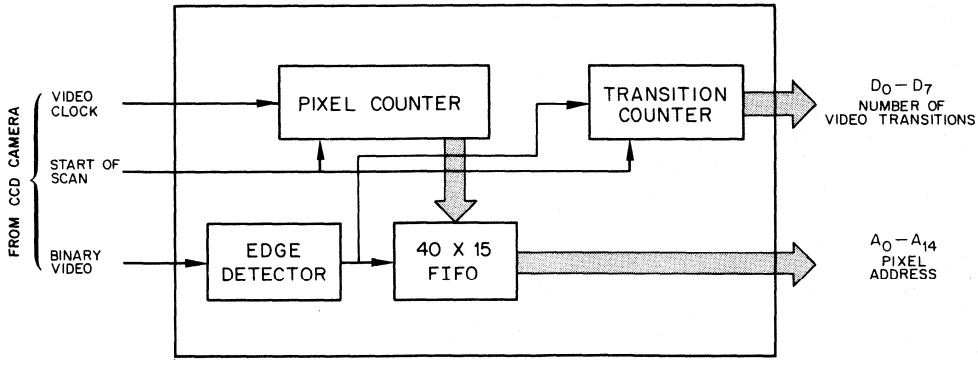
The Pixel Locator is an optional accessory which can be ordered for use with any of the Fairchild standard-product Line Scan Camera Subsystems; the 256-element CCD1100, the 1024-element CCD1300 or the 1728-element CCD1400.

The accessory is a single printed circuit board which is installed in a 3" X 6" X 10" enclosure designed as a companion to the control unit with the standard subsystem family. All required bias voltage and camera signal input connections are made by a single 15-wire cable which is provided for interconnection between the Pixel Locator and control unit. A mating 50-pin connector is provided to allow user construction of a cable for accessing of the Pixel Locator I/O ports.

The primary electrical function of the Pixel Locator is generation of a set of digital output data words which indicate the pixel address locations where white-to-black and black-to-white transitions occur in the Binary Video signal from the associated Line Scan Camera. A pixel is a "picture element", which physically corresponds to a discrete photosite in the monolithic Charge Coupled Device image sensor employed for optical detection in the camera. There are 256 pixels (and hence 256 corresponding pixel addresses) in the CCD1110 camera, 1024 pixels in the CCD1310, and 1728 pixels in the CCD1410.

First-In First-Out buffer memory storage is provided for the set of address words detected by the Pixel Locator, which allows the users system to access address data at any rate up to 2M words per sec. The sequentially-available set of digital address output words permits many non-contact measurement application problems to be resolved with simple binary subtraction or digital display circuitry.

As a secondary function, the Pixel Locator also provides an 8-bit output word which indicates the number of video signal transitions which were detected in a preceeding camera line scan readout.



PIXEL LOCATOR BLOCK DIAGRAM

FAIRCHILD
A Schlumberger Company

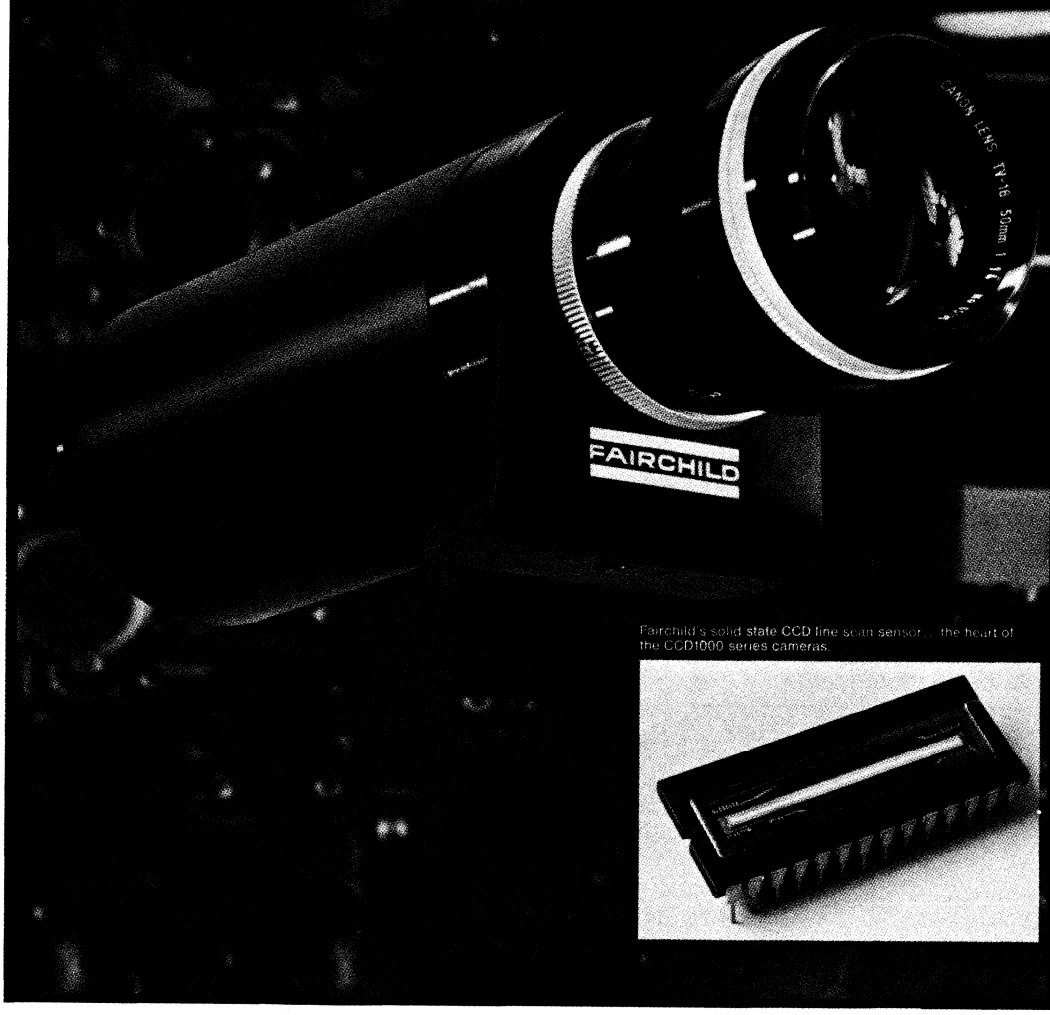
CCD

FAIRCHILD
A Schlumberger Company

CCD1000 Series Industrial Line Scan Cameras

CCD Cameras for Non-Contact Measurement and Inspection...

...at the Leading Edge of Technology



Fairchild's solid state CCD line scan sensor... the heart of the CCD1000 series cameras.

Industrial Line Scan Cameras CCD1200R 512-Element CCD1300R 1024-Element CCD1500R 2048-Element

CCD Imaging

Description

Fairchild Models CCD1200R, CCD1300R, CCD1500R are rugged line scan cameras designed for incorporation into non-contact electro-optical measurement and process control systems. The model CCD1200R has a resolution of 512 elements per line; the model CCD1300R has a resolution of 1024 elements per line; and the model CCD1500R has a resolution of 2048 elements per line.

The small sealed enclosure permits the camera to be used in systems where space is limited. The camera can be installed in a water jacket when necessary for environmental protection, and can be located more than 200 cable feet away from a control unit/power supply. A C-mount lens adaptor is standard for the CCD1200R and CCD1300R cameras; a T-mount adaptor is standard with the 2048 element model CCD1500R.

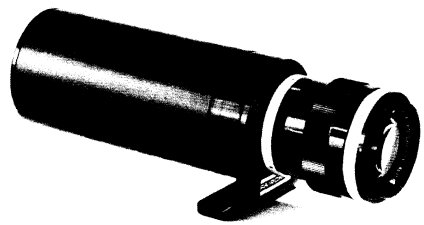
Only two clock signals input through high noise immunity differential line receivers are required for control of the line scan function in the camera. A data rate clock, which can have a frequency of up to 20 MHz, determines the frequency at which video data is read out of the camera: an exposure control clock determines the line scanning rate of the camera. Data rate and exposure clock echo signals are output from the camera for control of system timing at the control unit of a system; these echo signals can be used for timing accommodation in systems using a longer cable between controller and camera. Twisted pair clock wiring can be used for most camera applications; shielded twisted pair cabling is recommended in electrostatically and electromagnetically noisy environments.

The cameras require power supply inputs of +5 and +15 Vdc. Internal regulators and filters provide noise immunity for the bias voltage inputs. Separate force and sense lines allow control of supply voltages and ground potentials at the camera end of long cables.

Two time-division multiplexed analog video outputs are available from coaxial connectors on the camera, at a 75 ohm source impedance. The output video data rate, when measured in pixels per second, is equal to the data rate clock input frequency. Video data is intended to be processed in user-designed circuitry in a control unit as required by the application; simple comparators are sufficient for typical width measurement applications which use black-white binary video while more elaborate analog and/or A-D converted processors are required for systems recognizing gray-scale.

Applications

- NON-CONTACT INDUSTRIAL MEASUREMENT & INSPECTION
- WIDTH/POSITION/DEFECT DETECTION IN PROCESS CONTROL SYSTEMS
- PATTERN RECOGNITION
- CHARACTER RECOGNITION
- IMAGE ANALYSIS FOR COMPUTER CONTROLLED APPLICATIONS



- SMALL, COMPACT SEALED ENCLOSURE
- WELL SUITED FOR USE IN RUGGED INDUSTRIAL ENVIRONMENTS
- ALL SOLID STATE
- UTILIZES CCD SENSOR: 512, 1024, 2048 RESOLUTIONS AVAILABLE
- REMOTE OPERATION (OVER 200 CABLE FT.)
- WATER JACKET COMPATIBLE FOR HIGH TEMPERATURE OPERATION
- TWO CLOCK INPUTS CONTROL CAMERA
- NO GEOMETRIC DISTORTION
- 1000:1 DYNAMIC RANGE
- ELECTRONICALLY VARIABLE DATA RATE AND EXPOSURE TIME
- ACCEPTS C-MOUNT OR 35 MM LENSES
- VIDEO DATA RATES UP TO 20 MHz
- SCAN RATES UP TO 40,000 LINES/SECOND

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CCD

CCD1200R/1300R/1500R

Ruggedized Camera Specifications

Camera	CCD1200R	CCD1300R	CCD1500R
Sensor	CCD153 512 x 1 Element Array	CCD133 1024 x 1 Element Array	CCD143 2048 x 1 Element Array
Photo Element Size	13 μm x 13 μm Located on 13 μm centers		
Geometric Distortion	Determined by lens selected		
Dynamic Range	Typically better than 1000:1, excluding clock coupling		
Dark Signal Non-Uniformity (DSNU)	50 mV P-P max. at an integration time of 8.33 ms and T_A = 25°C		
Photoresponse Non-Uniformity (PRNU)	100 mV P-P max. @ 1 V V_{OUT}, measured at T_{INT} = 8.33 ms, T_A = 25°C, using a daylight fluorescent light source		
Saturation Exposure	Typically 0.67 μJ/cm^2, using a daylight fluorescent lamp light source		
Saturation Signal Voltage	2 V P-P typical, 1 V P-P minimum (UNTERMINATED)		
Spectral Response	The camera includes a Corning 1-75 filter		
Video Data Rate	20 M pixels per second maximum (typical)		
Exposure Time (Min)	26 μS	52 μS	103 μS
Scan Rate (Max) Lines/Second	38 K	19 K	9.7 K

Maximum usable exposure time is limited by the dark signal level developed during the integration time. Dark signal level is an exponential function of camera and (consequently sensor) temperature: dark signal level doubles for each 6-8°C rise in temperature. Dark signal level also increases linearly with exposure time.

Functional Description
As is shown by the block diagram, the circuitry within the camera is comprised of logic and driver control of the CCD image sensor, the sensor itself, video buffers and power supply filters. An infra-red reject optical filter and lens mounting adaptor are included in the enclosure.

Image Sensor
The Charge Coupled Device line scan image sensor used in the camera is a monolithic component containing a single row of image sensing elements (photosites or pixels), two analog transport shift registers, and two output sense amplifiers. Light energy falling on the photosites generates electron charge packets which are proportional to the product of exposure time (1 ÷ line scan frequency) and incident light intensity. The photosite charge packets are transferred in parallel to the two analog transport registers in response to an exposure time clock signal input into the camera. The transport registers, in response to the data rate clock, deliver the packets in sequence to an integrated charge sensing amplifier where they are converted into proportional video signal voltage levels.

The model CCD1200R camera uses a selected version of the 512 element Fairchild CCD153 sensor; the model CCD1300R camera uses a selected version of the 1024 element CCD133 sensor; and the model CCD1500R uses a selected version of the 2048 element CCD143 sensor.

The key advantages of Fairchild's isoplanar buried channel CCD sensors for use in the line scan cameras include high data rate capability, high charge transfer efficiencies, low noise, relatively small die sizes, and geometrically precise construction.

Logic and Drivers
Differential line driver input signals are converted into TTL level voltages by the line receivers, and then amplified and shaped for control of the image sensor clock inputs. Single-ended TTL clock inputs can be used if the negative differential input is biased at +1 V; this technique is recommended only for short cable clock inputs and/or relatively slow video data rate operation.

The frequency of the data rate clock input signal determines the rate at which charge packets are transported along the CCD analog shift register. Valid video data from odd-numbered sensor photosites becomes available within 50 ns following a falling edge of a data rate clock signal from camera video output A; the signal from video output connector B becomes valid 50 ns after the rising edge of an input data rate clock.

A positive exposure control input signal causes accumulated photosite data to be transferred within the CCD to the analog transport registers for readout under control of the data rate clock. The interval between exposure control inputs is the sensor exposure time.

As is noted in the timing diagram, the exposure control pulse input width is unimportant for camera operation. The data rate and exposure control inputs need not be synchronized. The only timing restriction is that the interval between exposure control input signals should be greater than the camera resolution (# of elements) times 1/video data rate to prevent addition of old and new charge packet data in the CCD registers.

Video Output Buffers
Sensor video is buffered by two independent unity-gain 75 ohm output impedance buffers to become the camera video outputs. The video signals ride on a dc level of about 4 volts above ground. External processing circuitry can be used to demultiplex the two video signals. The amplitude of each video signal will typically be 1 V P-P at sensor saturation; the video signal waveforms are sampled and held continuous signals with a small high-frequency sampling clock content.

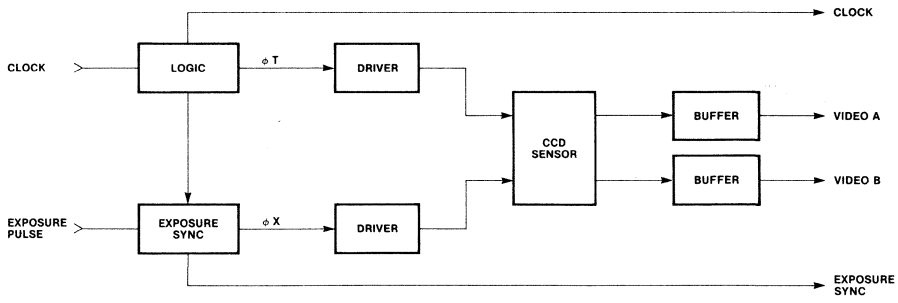
Optical Components
Each photosite in the sensor is 13 microns (0.51 mils) square. Total active array length is 3.3 mm (.131 inches) for the model CCD1200R, 13.3 mm (.52 inches) for the model CCD1300R, and 26.6 mm (1.04 inches) for the model CCD1500R.

The 512 and 1024 element array lengths are compatible with C-mount lens. The 2048 element array should be used with a 35 mm film camera format lens. Various focal length lenses can be provided by Fairchild as camera accessories.

When ordering, specify device type LENS25C for 25 mm; LENS50C for 50 mm, standard C-mount lens.

A Corning type 1-75 infra-red absorption filter is made a part of the standard cameras. The filter transmission convolved with the spectral responsivity of a silicon CCD sensor gives the camera a response ranging from about 400 to 800 nm, with a peak response at about 700 nm.

Block Diagram



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CCD

CCD1200R/1300R/1500R

Camera Connections

J1

Name	Pin
MC1⁺	6
MC1⁻	13
XTO⁺	5
XTO⁻	12
MC2⁺	8
MC2⁻	15
XT2⁺	7
XT2⁻	14
+5 FORCE	4
+5 SENSE	11
+15 FORCE	2
+15 SENSE	9
GND FORCE	3
GND SENSE	10
GND SHIELD	1

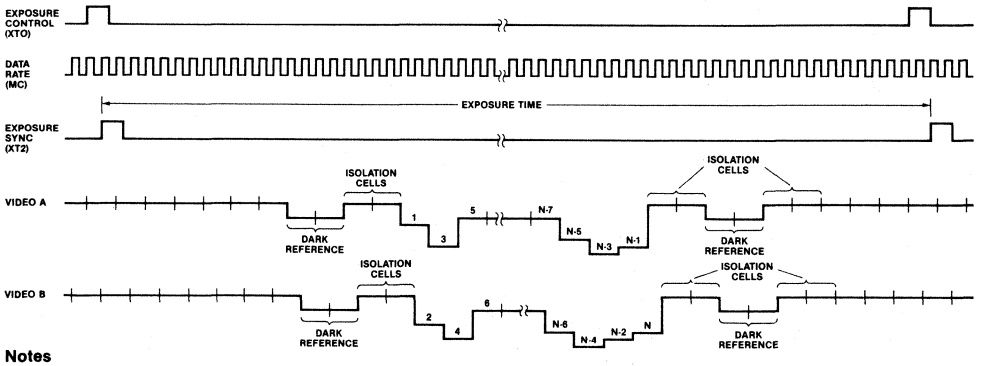
J3 VIDEO A J4 VIDEO B

Inputs:
- Data Rate Clock (MC1), 20 MHz MAX, Differentially Received
- Exposure Control Clock Pulse (XTO), 25ns Min. Width, Differentially Received
- +5 V @ 500 mA MAX
- +15 V @ 250 mA MAX
- Ground

Outputs:
- Data Rate Clock (MC2), Differentially Driven
- Exposure Sync (XT2), Differentially Driven
- Video A, 75 Ohm Source Impedance
- Video B, 75 Ohm Source Impedance
- +5 V Sense
- +15 V Sense
- Ground Sense

Dimensions:
- Diameter 2.25″
- Length 5.125″ Without Lens

Timing Diagram



Notes

N = Number of elements in the array, i.e., 512, 1024, or 2048

XTO = At least 25 ns width, may be asynchronous and should not occur while video data is being clocked out

MC = 20 MHz MAX. Data rate out equals data rate in plus 50 ns (typical camera propagation time) and any transmission line delay

XT2 = Time interval between leading edges determines integration time

Ordering Information

When ordering, specify device type

CCD1200R	CCD1300R	CCD1500R
512 x 1 Element Array	1024 x 1 Element Array	2048 x 1 Element Array

For further information please call your nearest Fairchild Sales Office. For technical or applications assistance call (415) 493-8001.

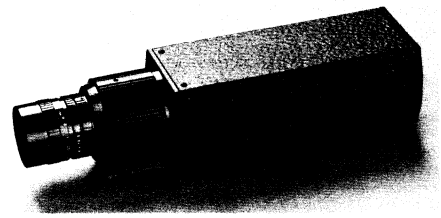
CCD3000
Video Communications Camera
Automation Camera Series

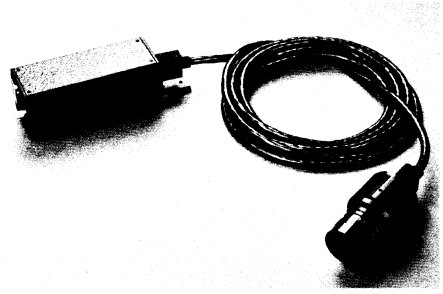
CCD Imaging

DESCRIPTION

The CCD3000 is a small, rugged, solid-state camera designed for use in industrial environments. The CCD3000 Video Communications Camera provides NTSC television video output signals for display of high-resolution images on standard monitors or for digital analysis using NTSC image processing equipment. The camera output is a 525-line, 2-field per frame, fully interlaced format with a resolution of 488 lines per frame by 380 elements per line.

The camera, as pictured, can be used as a single piece unit or separated into a camera control unit and sense head connected by a flexible cable. The small, rugged, lightweight sense head is designed to tolerate high accelerations and vibrations which, for example, might be encountered on a quickly moving robot arm.

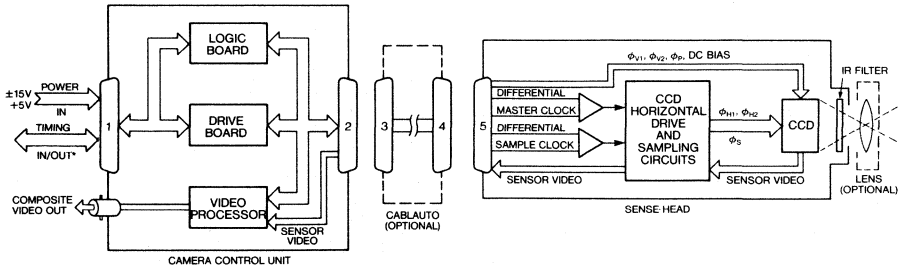




FEATURES

- **SMALL, COMPACT ENCLOSURES WITH SEALED REMOTABLE SENSE HEAD.**
- **WELL SUITED FOR USE IN RUGGED INDUSTRIAL ENVIRONMENTS.**
- **ALL SOLID-STATE.**
- **SELF-CONTAINED (ONLY DC POWER INPUT REQUIRED).**
- **HIGH RESOLUTION BURIED-CHANNEL CCD.**
- **NO LAG OR GEOMETRIC DISTORTION.**
- **WIDE DYNAMIC RANGE: TYPICALLY 1000:1.**
- **ELECTRONICALLY VARIABLE FRAME RATES.**
- **GEN-LOCK CAPABILITY.**

CCD3000 BLOCK DIAGRAM



1 — 25 PIN D CONNECTOR
2, 3, 4, 5 — 31 PIN D CONNECTOR

* OPTIONAL

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CCD

CCD3000

SPECIFICATIONS

Scanning Format — Interlaced 2 field per frame, 380 elements per line is standard. (Non-interlaced 1 field per frame is a pc strap option.)

Scan Timing — Frame rate is 30Hz, data rate is 7.16M elements per second under control of internal crystal-controlled oscillator.

Synchronization — Can be gen-locked with horizontal and vertical drive signal inputs.

Output Signals — Analog Video: 1.4 Vp-p Composite, 75 ohm, Sync (0.4Vp-p) Negative, Black = 0 ± .1V. (Sync removable with pc strap.) Timing: Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock.

Resolution — 488 lines per picture height, 380 lines per picture width.

Sensor — Monolithic Silicon CCD. Element spacing: 18μm C-C vertical, 30μm C-C horizontal. Aspect Ratio: 4:3 (horizontal:vertical). Image Diagonal: 14.4mm.

Dynamic Range — 1000:1.

Saturation Irradiance — 8.4μW/cm^2 at normal scan rate.

Minimum Illumination — Useable Picture at 5 lux with an f/1.4 lens.

Contrast Transfer Function, Horizontal — 75% at 380 lines/picture width.

Contrast Transfer Function, Vertical — 70% at 488 lines/picture height.

Lens — C-mount is standard 1" Vidicon types are recommended. (See Options.)

Cosmetic Performance* — (At $T_A = 25°C$)
DSSNU ≤ 20 mVp-p (≤2% Peak Output)
PRSNU ≤ 5% V_{OUT}
Number of Blemished Elements ≤100 pixels
Largest Dimension of Blemished Area ≤3 contiguous elements
Number of Blemished Columns = 0

Enclosure — Sense head is gasket and O-ring sealed.

Dimensions — See figure.

Weight — Sense Head: ≤8 oz., Sense Head and Control Unit: 2.2 lbs.

Environmental Conditions — Operating Ambient Temperature: 0-50°C. Acceleration and Shock: >100G, any axis. Vibration: 20-2000Hz, 20G, any axis.

Power Requirements — <10W input, ±15, +5Vdc.

***Notes**

1. These characteristics are measured at uniform illumination levels providing video signal output levels from 0V (Black) to 1.0Vp-p (Full White).
2. Blemished elements are contained in randomly located small (not larger than 3 × 3 elements) areas where the video output signal differs from the output of the surrounding area by >±100mV.
3. Certain video anomalies may sometimes be observed in the displayed camera output when the sensor illumination level exceeds the light level needed to achieve the normal camera saturation output video signal level of 1.0Vp-p.
4. The amplitude of DSSNU and the output of all sensor elements in the dark should be expected to double for each 5-10 degree C increase in sense head temperature.
5. Cameras with improved or degraded cosmetic performance specifications are available to volume purchasers with price adjustments. Please consult the factory for more information.

FUNCTIONAL DESCRIPTION

The CCD3000 camera is shipped as a single-piece unit comprised of a sense head and camera control unit connected by a dovetail member. These two subunits may be separated by an optional 12-foot cable permitting remote operation of the sense head. (See Options Section of Data Sheet). Each section contains electronics as illustrated in the two block diagrams.

Image Sensor

The image detector used in the CCD3000 camera sense head (See Block Diagram) is a selected Fairchild CCD222; a monolithic 488X380-element charge-coupled device (CCD) image sensor. The buried channel CCD architecture employed in the sensor minimizes noise and allows high frame rates without sacrificing charge transfer efficiency. The advanced Fairchild CCD technology allows the camera to offer zero lag and geometric distortion, lower power consumption, small size, and unusual robustness for use in industrial environments.

Sense Head

The sense head contains the image sensor and circuitry for generating the high frequency horizontal register and sample pulse clock signals for CCD control and a buffer for the sensor video. All other CCD timing and drive electronics, supply and bias voltages as well as video processing electronics are contained in the camera control unit. Light reaching the sensor is filtered by a 2.0mm thick Schott BG-38 glass in order to eliminate IR content and give a near photopic spectral sensitivity. The sensor is rigidly held in position and precisely aligned with respect to the sense head mounting foot. The sensor is thermally connected to the exterior walls at the sense head by low thermal resistance hard-anodized aluminum internal structures. The sense head is sealed by O-rings, gaskets, and by bonding of the filter glass into the lens mount.

Camera Control Unit

The camera control unit houses three pc cards performing the functions of camera and sensor timing control, CCD drive and video processing, interconnected by two pc mother boards. Camera timing is controlled by an internal 14.318MHz master clock oscillator located on the drive board. The frequency of this oscillator is controlled by a phase locked loop circuit when the camera timing is "gen-locked" to external vertical and horizontal drive signals.

Timing waveforms for sensor drive and sync signals for the

formation of NTSC composite video are derived from the master clock signal. These timing signals are then fed to the drive board where the TTL level signals are altered to CCD drive level signals required to operate the sensor. From the drive board, sensor clocks are fed through the 31-pin D connector to the sense head and the composite sync signal is forwarded to the video processor board.

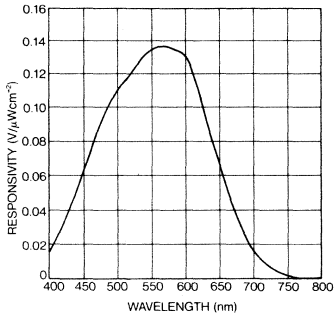
The video processor receives sensor video from the CCD in the sense head. The video is line clamped, amplified, and blanked with composite blanking from the logic board, and then summed with the composite sync signal from the drive board to yield the RS170 composite video at the BNC output at the back of the camera. Timing waveforms as well as sensor video are provided at the 25-Pin D connector at the back of the camera (See Pin Diagram).

Power

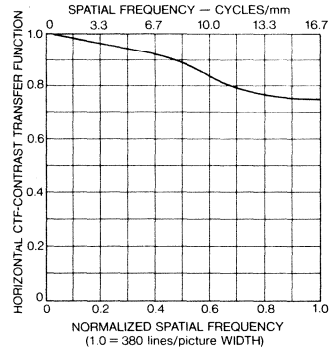
The cameras require inputs of ±15 and +5Vdc. Regulators on-board provide all voltage levels needed to drive the amplifiers and various clocks.

TYPICAL PERFORMANCE CURVES

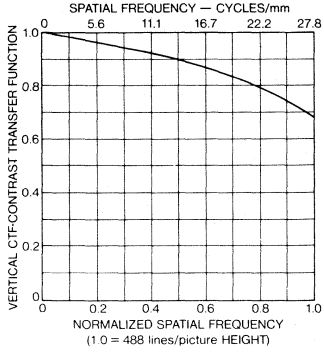
TYPICAL SPECTRAL RESPONSE



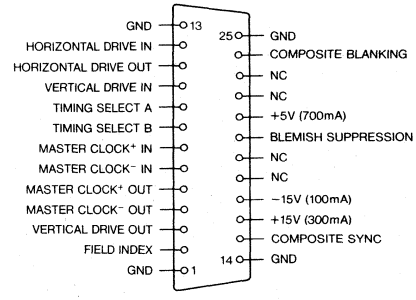
HORIZONTAL CONTRAST TRANSFER FUNCTION



VERTICAL CONTRAST TRANSFER FUNCTION



I/O PIN CONNECTIONS

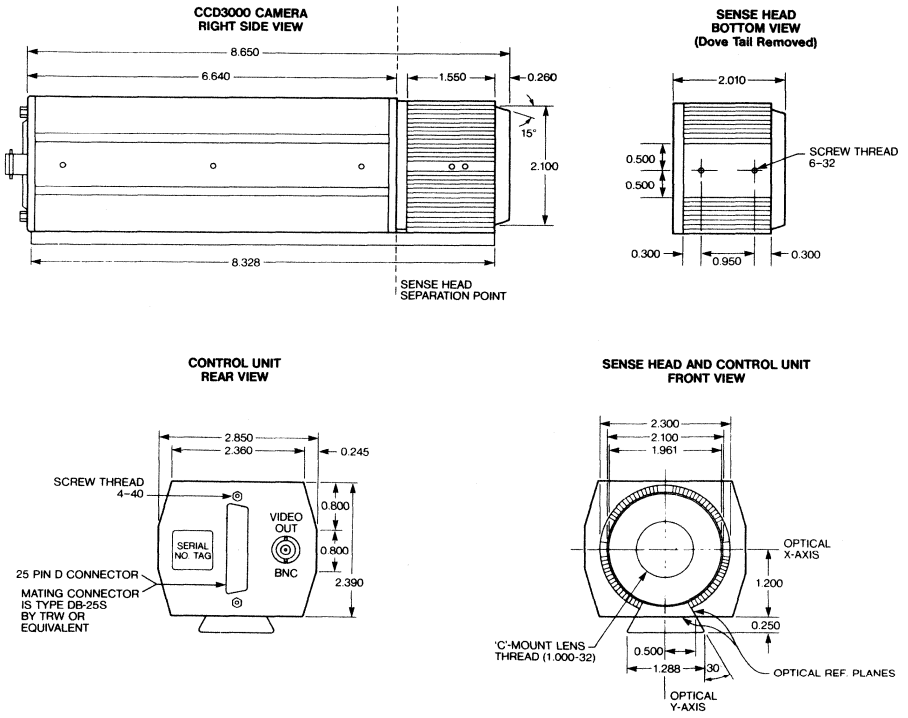


MATING CONNECTOR IS TYPE DB-25S BY TRW OR EQUIVALENT

CCD3000

MECHANICAL DIMENSIONS

(Note: All dimensions are in inches)



OPTIONS AND ORDER INFORMATION

CCD3000 — Includes camera, power supply unit, and remote sense head cable.

CAM3000 — CCD3000 less power supply unit and remote sense head cable.

Power Supply Unit — This unit provides ±15 and + 5Vdc bias voltage inputs to the CCD3000 derived from power line voltages of 120±10 or 240±20Vac, 47-63Hz. The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive and horizontal drive input and output signals and an external clock input as TTL levels. The rear panel contains connectors for interfacing the camera and power supply to the VIP100 Video Interface Processor. A 6' (approx. 2m) cable is provided for interconnection of the camera control unit and the power supply. To order, specify Model PWRSPLY.

Remote Sense Head Cable — Allows sense head to be remoted from camera control unit by a distance of 12' (approx. 4m). To order, specify Model CABLAUTO.

Lenses — 1" Vidicon type 'C'-mount lenses are available in focal lengths of 13mm, 25mm and 50mm. To order, specify Models LENS13C, LENS25C and LENS50C, respectively.

Monitor — NTSC monitor. To order, specify Model MONITOR.

CCD 3000F
Video Communications Camera With Fiber Optic Faceplate

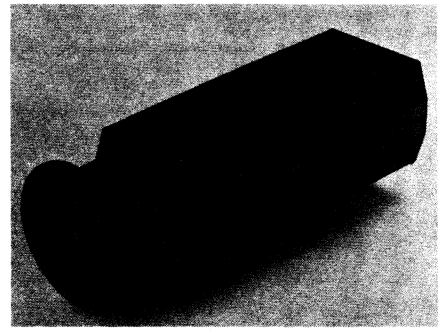
CCD Imaging

DESCRIPTION

The CCD3000F is a small, rugged, solid state camera capable of accepting fiber optic inputs. The camera provides video output signals for display of high-resolution images on NTSC standard monitors or for digital analysis using RS170A-compatible image processing equipment.* The sense head of the CCD3000F features a fiber optic faceplate and mounting flange which makes it ideal for interfacing to customer fiber optic image inputs. The fiber optic coupling can dramatically increase the efficiency of image input in comparison to normal lens image forming systems. This feature makes the CCD3000F well suited for applications in streak cameras, large-format intensifier cameras, X-ray and UV imaging, endoscopy and other medical imaging applications, in addition to numerous scientific and industrial automation applications.

The CCD3000F camera incorporates a CCD222 image sensor with a resolution of 488 lines per frame by 380 elements per line. The standard glass cover on the CCD222 has been replaced with a fiber optic faceplate, composed of a stack of clad glass fibers fused together in a parallel array. The extramural-absorption (EMA) cladding, which minimizes internal flare, is utilized as the optical insulation between the fibers as well as to bond the fibers together. The center-to-center spacing of the optic fibers is approximately 6μm.

The types of glasses used in the faceplate provide a very large acceptance angle for the entering light; the nominal numerical aperture of the faceplate is 1.0. The fiber optic faceplate is in optical contact with the top surface of the area sensor die but physically separated from it by a thin layer of optical immersion oil with N_D of 1.515. The faceplate is held securely with the aid of an anodized metal frame.

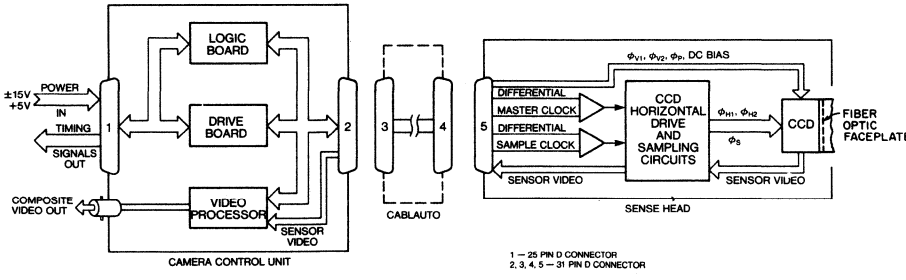


FEATURES

- FIBER OPTICS INPUT, NA = 1.0, WITH EMA.
- FLANGE COUPLING FOR EASE OF INTERFACING.
- COMPLETE SYSTEM, INCLUDING POWER SUPPLY.
- SPRING LOADED SENSOR MOUNTING.
- ALL SOLID-STATE.
- SMALL AND COMPACT.
- HIGH RESOLUTION BURIED-CHANNEL CCD.
- GEN-LOCK CAPABILITY.

*NOTE: As the CCD3000F is based on the CCD3000 video communications camera, please refer to the CCD3000 data sheet for a more detailed description. The CCD3000I, an intensified version of the CCD3000F, is also described under separate cover.

CCD3000F BLOCK DIAGRAM



FAIRCHILD
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CCD

CCD3000F

PERFORMANCE SPECIFICATIONS

The cosmetic performance of a CCD3000F may be slightly inferior to that of a CCD3000 because of blemishes within the fiber optic faceplate. The dimension of any one blemished area on the CCD3000F camera will not exceed 4 contiguous pixels. Shear distortion in the fiber bundle will not optically displace any sensor pixels by more than ±½ the sensor's pixel-to-pixel spacing. PRSNU (Photo Response Shading Non-Uniformity) will not increase by more than 3% of V_{OUT}. The MTF (Modulation Transfer Function) at 380 columns/picture width will be higher than 70%, while the MTF at 488 horizontal lines/picture height will exceed 65%.

RECOMMENDED TEMPERATURES

Operating:	0 — 40°C
Storage:	0 — 60°C

COUPLING TO FIBER OPTIC FACEPLATE

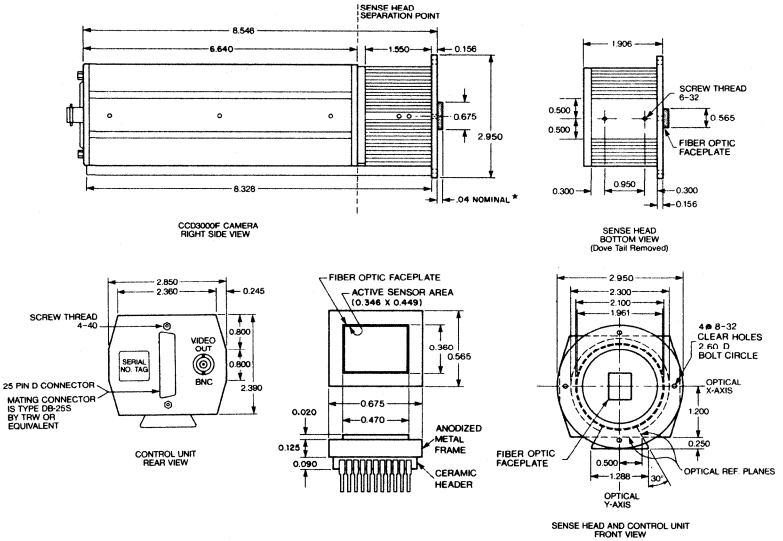
The camera unit can best be interfaced via a flange 2.95" in diameter. The sensor mounting board which contains a socket for mounting the CCD222 fiber optic device is spring loaded providing approximately 200g of force against the mating fiber optic surface. It is recommended that a drop of immersion oil be used at this fiber optic interface for best coupling.

FACEPLATE CARE

The fiber optic faceplate can be cleaned with mild detergent or organic solvent. Drying should be preceded by a wetting agent to prevent water spotting. Wiping dry must be done with lens tissue or equivalent to prevent scratching of the polished glass surfaces. The extreme pressures created by edge contacts can chip the camera faceplate or mating fiber optics bundles. Care should be exercised when interfacing the camera faceplate to user-supplied mating optics.

MECHANICAL DIMENSIONS

(NOTE: All dimensions are in inches)



*NOTE: The spring-loaded faceplate will move inward approximately 0.06 inches in response to an applied force normal to the faceplate of 0.90 kg.

OPTIONS AND ORDER INFORMATION

To order the CCD3000F camera, please use the appropriate ordering code from the table below:

Order Code	Description
CCD3000F	Includes camera with fiber optic faceplate, power supply unit, and remote sense head cable.
CAM3000F	CCD3000F less power supply unit and remote sense head cable.
Monitor	NTSC monitor.

For further information on CCD products, call your nearest Fairchild sales office, representative or distributor. For engineering assistance call (415) 493-8001 (TWX 910-373-2110) or write Fairchild CCD Imaging, 3440 Hillview Ave., Palo Alto, CA 94304.

PRELIMINARY

VIDEO COMMUNICATIONS CAMERA
AUTOMATION CAMERA SERIES
CCD3001

DESCRIPTION

The CCD3001 is an improved version of the CCD3000 automation camera offering additional features of element anti-blooming, greater flexibility in timing control, lower power consumption and a more flexible, noise-protected remote sense head cable.

The CCD3001 is a small, rugged, solid-state camera designed for use in industrial environments. The CCD3001 Video Communications Camera provides NTSC television video output signals for display of high-resolution images on standard monitors or for digital analysis using NTSC image processing equipment. The camera output is a 525-line, 2-field per frame, fully interlaced format with a resolution of 488 lines per frame by 380 elements per line.

The camera can be used as a single piece unit or separated into a camera control unit and sense head connected by a flexible cable. The small, rugged, light-weight sense head is designed to tolerate high accelerations and vibrations which, for example, might be encountered on a quickly moving robot arm.

The camera is supplied with either a gen-lock circuit accepting separate horizontal and vertical drive inputs (CCD3001) or a ciruit accepting a composite sync or composite video input (CCD3001S).

SPECIFICATION SUMMARY

Camera Output Format: RS170A standard 30 frame per second, 2 interlaced fields per frame. (Frame rate can be controlled by input of external master clock signal if desired).

Scanning Format: Interlaced 2 field per frame, 483 line per frame, 380 element per line is standard. User options allow scanning at non-interlaced 244 line per frame, or psuedo-interlaced scanning with 360≈line per picture height resolution and exposure times of 1/60 second.

Synchronization and timing control: Standard CCD3001 can be synchronized (gen-locked) with horizontal and vertical drive inputs. Model CCD3001S can be synchronized (gen-locked) with composite sync or composite video input.

Output Signals:

Analog Video: Composite 0-1.4 Vp-p, Black=0V, Sync=-0.4V, 75 ohms.

Timing: Vertical and Horizontal sync, composite sync and blanking, field index, data rate clock as TTL levels. Master clock as differential signal.

Resolution: 488 lines per picture height, 380 lines per picture width.

Sensor: Monolithic buried channel CCD, 488x380 elements, interline transfer organization, with element anti-blooming.

Element Spacing: 18 µm c-c vertical, 30 µm c-c horizontal.

Aspect Ratio: 4:3 (horizontal: vertical)

Input Signals: (At user's option) Vertical and horizontal drive for gen-lock (composite video or sync with model CCD3001S), timing mode selects, differential master clock.

Dynamic Range: 1000:1 (peak signal: temporal noise)

Saturation Irradiance: 8.4µW/cm^2 at normal scan rate.

Unusual Features: Exposure can be extended in field interval increments for increased sensitivity, special timing for flash exposures.

Enclosure: Both camera pieces are gasket and O-ring sealed.

Dimensions:

As 1-Piece Camera: 8.7" long, 2.4" high, 2.8" wide.
As 2-Piece Camera: Remote Sense Head: 2.3" diameter, 2.0" long. Camera Control Unit: 6.7" long, 2.4" high, 2.8" wide.
Power Supply: 8" wide, 3" high, 6¼" deep.
Sense Head to Camera Control Unit Cable: 12' standard length is included.
Weight: Sense Head: ≤ 8oz., Sense Head and Control Unit: 2.2lbs.

Environmental Conditions: Operating Ambient Temperature: Sense Head: 0-50°C. Control Unit: 0-50°C. Acceleration and Shock (Sense Head) : > 100G, any axis. Vibration: 0-2000Hz, 2G, any axis.

Power Requirements for Camera: 5W input, ±15, +5 VDC. These requirements are met by the power supply unit.

Lens: Camera accepts C-mount lenses, 1" Vidicon types are recommended. Lens is optional.

PRELIMINARY

VIDEO COMMUNICATIONS CAMERA WITH FIBER OPTIC FACEPLATE

CCD3001F

The CCD3001F is an improved version of the CCD3000F solid state camera. The cameras are similar except for the new model (CCD3001F) is based on the CCD3001 camera which offers additional features of element anti-blooming, greater flexibility in timing control, lower power consumption and a more flexible, noise-protected remote sense head cable.

The CCD3001F, like the CCD3000F, features a fiber optic faceplate and mounting flange which makes it ideal for interfacing to customer fiber optic inputs. This feature makes the camera well suited for any applications using input from flexible coherent fiber optic bundles including X-ray and UV imaging, endoscopy, low light level imaging, as well as numerous scientific and industrial automation applications.

For further information on the CCD3001F camera please refer to either the CCD3000F or preliminary CCD3001 data sheet.

FAIRCHILD
A Schlumberger Company

CCD

PRELIMINARY

INTENSIFIED VIDEO COMMUNICATION CAMERA
AUTOMATION CAMERA SERIES
CCD3001I

The CCD3001I is a solid state camera utilizing a microchannel wafer image intensifier for industrial and scientific applications requiring low-light level capability. The camera provides video output signals for display of high-resolution images on NTSC standard monitors or for digital analysis using RS170A-compatible image processing equipment. The image input to the intensifier is through a C-mount lens. The amplified intensifier output is coupled to the CCD image sensor by coherent fiber optics. Typical uses are in biological and medical applications for acquisition of low-light level data through microscope optics, automatic alignment systems for semiconductor masking procedures and surveillance applications in dimly illuminated areas.

The CCD3001I, based on the CCD3001 video communications camera, is likewise supplied with either a gen-lock circuit accepting horizontal and vertical drive inputs (CCD3001I) or one accepting a composite sync or composite video input (CCD3001IS).

SPECIFICATION SUMMARY

The CCD3001I incorporates all the same features and meets all the specifications of the CCD3001 except for the following:

Sensor: Microchannel wafer intensifier coupled to a CCD image sensor by effecient fiber optics.

Intensifier: 18mm second generation tube with 520 "extended red" response photocathode, proximity focused ruggedized construction and assembly.

CCD: Monolithic buried channel, 488x380 elements, interline transfer organization, with element anti-blooming, proximity-coupled fiber optics input faceplate.

Resolution: Limiting resolution $\geq$25 lp/mm

Sensitivity: Usable image detection at $\leq 10^{-3}$ lux scene illumination, F1.4 lens.

Automatic Brightness Control: Intensifier power supply saturation provides wide range automatic light level control.

Dimensions: As 1-Piece Camera: 10" long, 2.4" high, 2.8" wide.

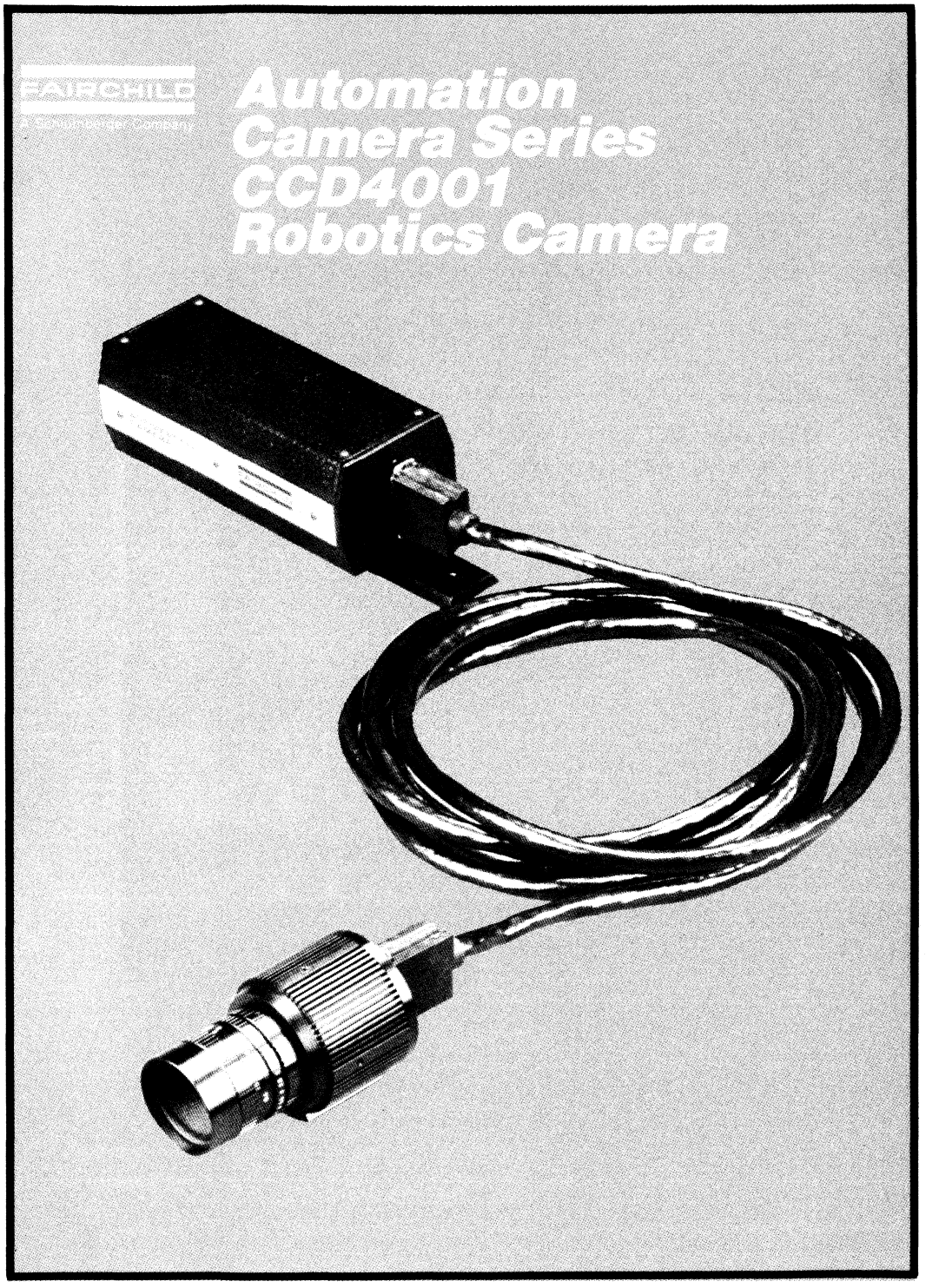
As 2-Piece Camera: Remote sense head: 2.3" diameter, 3.3" long.
Camera Control Unit: 6.7" long, 2.4" high, 2.8" wide.

Weight: Sense Head: 12oz., Sense head and control unit: 2.2 lbs.

Environment Conditions: Operating Ambient Temperature: Sense Head: 0-50°C. Control Unit: 0-50°C. Acceleration and Shock (Sense Head): > 20G, any axis.

FAIRCHILD
A Schlumberger Company

CCD



Robotics Camera CCD4001

The Fairchild CCD4001 is a rugged self-contained camera which makes it easy for industrial users to take advantage of the inherent geometric accuracy, wide dynamic range and reliability of a buried-channel charge coupled device image sensor. The CCD4001 provides image data output in a non-interlaced 256 × 256 element square pixel pitch format which can be efficiently utilized by a CPU for automatic inspection, recognition and robot guidance. The camera image output may also be displayed on standard monitors. In this format, the camera output is a 525-line, interlaced format with a resolution of 256 lines per field by 256 elements per line. Each frame of video is composed of two identical fields.

The camera, as pictured, can be used as a single-piece unit or separated into a camera control unit and sense head connected by a flexible cable. The small, rugged, lightweight sense head is designed to tolerate high accelerations and vibrations which, for example, might be encountered on a quickly moving robot arm.

Specification Summary

Sensor Scanning Format: Non-interlaced 256 elements per line, 256 lines per frame.

Sensor Scan Timing: Field rate is 60Hz.

Camera Output Format: Interlaced 2 identical fields per frame.

Camera Output Timing: NTSC compatible frame is 30Hz, data rate is 6.14M elements per second under control of an internal, crystal-controlled oscillator. (External clock input may be accepted for variable frame rates).

Synchronization: May be gen-locked with horizontal and vertical drive signal inputs. Also the scan rate may be controlled by clock input; frames can be synchronized by field index input.

Output Signals: Analog Video: 1.0V p-p Non-composite, 75 ohm, Black = 0 + 0.1V (Sync may be added with pc strap.) Timing: Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock, Video Valid.

Resolution: 256 lines per picture height, 256 lines per picture width.

Sensor: Monolithic silicon CCD. Element spacing: 22μm C-C horizontal; 22μm C-C vertical. Aspect Ratio: 1:1 (horizontal: vertical). Image Diagonal: 7.94mm.

Input Signals: (At user's option) Timing: Vertical and Horizontal Drive, Timing Mode Selects, Master Clock, Field Index.

Dynamic Range: 1000:1.

Saturation Irradiance: 6.0μw/cm^2 at normal scan rate.

Enclosure: Both camera pieces are gasket and O-ring sealed.

Dimensions:
As 1-Piece Camera: 8.7" long, 2.4" high, 2.8" wide.
As 2-Piece Camera: Remote Sense Head: 2.3" diameter, 2.0" long. Camera Control Unit: 6.7" long 2.4" high, 2.8" wide.
Power Supply: 8" wide, 3" high, 6¼" deep.
Sense Head to Camera Control Unit Cable: 12' standard length is included.
Weight: Sense Head: ≤8 oz., Sense Head and Control Unit: 2.2 lbs.

Environmental Conditions: Operating Ambient Temperature: Sense Head: 0-50°C. Control Unit: 0-50°C. Acceleration and Shock (Sense Head): >100G, any axis. Vibration: 0-2000 Hz, 2G, any axis.

Power Requirements for Camera: 5W input, ±15, +5 VDC. These requirements are met by the power supply unit.

Lens: Camera accepts C-mount lenses, 1" Vidicon types are recommended. Lens is optional.

Options and Order Information

Order Code	Description
CCD4001	Includes camera, power supply unit, interconnect cable and remote sense head cable.
CAM4001	CCD4001 less power supply unit, interconnect cable and sense head cable.
PWRSPLY	Power Supply Unit for CCD4001
CABL4001	Remote Sense Head Cable for CAM4001
Lenses	1" Vidicon type C-mount lenses are available in focal lengths of 13mm, 25mm and 50mm.
Monitor	NTSC monitor

FAIRCHILD
A Schlumberger Company

CCD

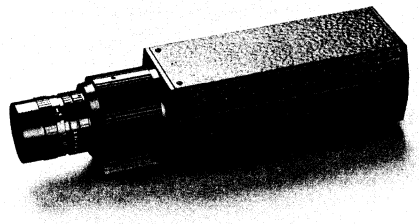
CCD4001
Robotics Camera
Automation Camera Series

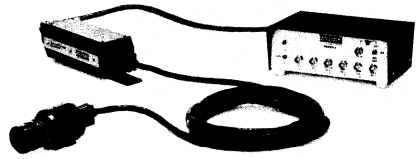
CCD Imaging

DESCRIPTION

The CCD4001 Robotics Camera is a small, rugged, solid-state camera designed for use in industrial environments. The CCD4001 incorporates a 256 × 256 element sensor with a square pixel pitch format. The camera can provide NTSC televison video output signals for display of images on standard monitors or for digital analysis using NTSC image processing equipment. The camera output is a 525-line, interlaced format with a resolution of 256 lines per field by 256 elements per line. Each frame of video is composed of two identical fields.

The camera can be used as a single piece unit or separated into a camera control unit and sense head connected by a flexible cable. The small, rugged, lightweight sense head is designed to tolerate high accelerations and vibrations which, for example, might be encountered on a quickly moving robot arm.

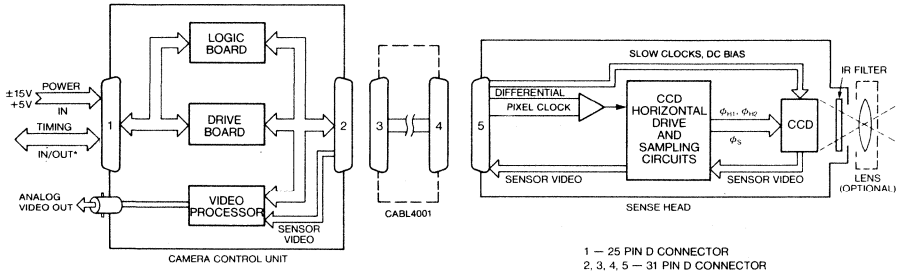




FEATURES

- **SMALL, COMPACT ENCLOSURES WITH SEALED REMOTABLE SENSE HEAD**
- **WELL SUITED FOR USE IN RUGGED INDUSTRIAL ENVIRONMENTS**
- **256 × 256 ELEMENT NON-INTERLACED SENSOR**
- **SQUARE PIXEL PITCH FORMAT**
- **ELEMENT BLOOMING CONTROL**
- **ALL SOLID-STATE, BURIED CHANNEL CCD**
- **SELF-CONTAINED**
- **NO LAG OR GEOMETRIC DISTORTION**
- **WIDE DYNAMIC RANGE: TYPICALLY 1000:1**
- **ELECTRONICALLY VARIABLE FRAME RATES**
- **GEN-LOCK CAPABILITY**
- **OPTIONAL EXTERNAL TIMING CONTROL**

CCD4001 BLOCK DIAGRAM



1 — 25 PIN D CONNECTOR
2, 3, 4, 5 — 31 PIN D CONNECTOR

* OPTIONAL USAGE

CCD4001

SPECIFICATIONS

Sensor Scanning Format — Non-interlaced 256 elements per line. 256 lines per frame.

Sensor Scan Timing — Field rate is 60Hz (using internal clock).

Camera Output Format — Interlaced 2 identical fields per frame.

Camera Output Timing — NTSC compatible frame rate is 30Hz, data rate is 6.14M elements per second under control of an internal, crystal-controlled oscillator. (External clock input may be accepted for variable frame rates.)

Synchronization — May be gen-locked with horizontal and vertical drive signal inputs. Also the scan rate may be controlled by clock input; frames can be synchronized by field index input.

Output Signals — Analog Video: 1.0V p-p Non-composite, 75 ohm, Black = 0 ± 0.1V (Sync may be added with pc strap.) Timing: Vertical and Horizontal Drive, Composite Sync and Blanking, Frame Index, Data Rate Clock, Video Valid.

Resolution — 256 lines per picture height, 256 lines per picture width.

Sensor — Monolithic silicon CCD. Element spacing: 22μm C-C horizontal; 22μm C-C vertical. Aspect Ratio: 1:1 (horizontal: vertical). Image Diagonal: 7.94mm.

Input Signals — (At user's option) Timing: Vertical and Horizontal Drive, Timing Mode Selects, Master Clock, Field Index.

Dynamic Range — 1000:1.

Saturation Irradiance — 6.0μw/cm^2 at normal scan rate.

Lens — Camera accepts C-mount lenses, 1" vidicon types are recommended. (See Options)

Cosmetic Performance* (At 25°C)

Dark Signal Shading Non-Uniformity (DSSNU) ≤20 mVp-p (≤2% Peak Output).

Photoresponse Shading Non-Uniformity (PRSNU) ≤5% of V_{OUT}.

Largest Dimension of Blemished Area ≤3 Continguous Elements

Number of Blemished Elements ≤100 pixels.

Number of Blemished Columns = 0

Enclosure — Sense head is gasket and O-ring sealed.

Dimensions — See Figure.

Weight — Sense Head: ≤8 oz., Sense Head and Control Unit: 2.2 lbs.

Environmental Conditions — Operating Ambient Temperature: Sense Head: 0-50°C. Control Unit: 0-50°C. Acceleration and Shock (Sense Head): >100G, any axis. Vibration: 0-2000Hz, 2G, any axis.

Power Requirements — 5W input, ±15, +5Vdc.

***Notes**

1. These characteristics are measured at uniform illumination levels providing video signal output levels from 0V (Black) to 1.0Vp-p (Full White).
2. Blemished elements are contained in randomly located small (not larger than 3 X 3 elements) areas where the video output signal differs from the output of the surrounding area by >±100 mV.
3. Certain video anomalies may sometimes be observed in the displayed camera output when the sensor illumination level exceeds the light level needed to achieve the normal camera saturation output video signal level of 1.0Vp-p.
4. The amplitude of DSSNU and the output of all sensor elements in the dark should be expected to double for each 5-10 degree C increase in sense head temperature.
5. Cameras with improved or degraded cosmetic performance specifications are available to volume purchasers with price adjustments. Please consult the factory for more information.

FUNCTIONAL DESCRIPTION

The CCD4001 camera is shipped as a single-piece unit comprised of a sense head and camera control unit connected by a dovetail member. These two subunits may be separated by a 12-foot cable (included with the camera) permitting remote operation of the sense head. A Power-Supply Unit is also included with the CCD4001 camera.

Each camera subunit contains electronics as illustrated in the block diagram.

Image Sensor

The image detector used in the CCD4001 camera sense head (See Block Diagram) is a selected, monolithic 256 X 256-element charge-coupled device (CCD) image sensor. The buried channel CCD architecture employed in the sensor minimizes noise and allows high frame rates without sacrificing charge transfer efficiency. The advanced Fairchild CCD technology allows the camera to offer low lag and geometric distortion, lower power consumption, small size, and unusual robustness for use in industrial environments.

Sense Head

The sense head contains the image sensor and circuitry for generating the high frequency horizontal register and sample pulse clock signals for CCD control and a buffer for the sensor video. All other CCD timing and drive electronics, supply and bias voltages as well as video processing electronics are contained in the camera control unit. Light reaching the sensor is filtered by a 2.0 mm thick Schott BG-38 glass in order to eliminate IR content and give a near photopic spectral sensitivity. The sensor is rigidly held in position and precisely aligned with respect to the sense head mounting foot. The sensor is thermally connected to the exterior walls at the sense head by low thermal resistance hard-anodized aluminum internal structures. The sense head is sealed by O-rings, gaskets and by bonding of the filter glass into the lens mount.

Camera Control Unit

The camera control unit houses three pc cards performing the functions of camera and sensor timing control, CCD drive and video processing, interconnected by two pc

CCD4001

mother boards. Camera timing is controlled by an internal 12.285MHz master clock oscillator located on the drive board. The frequency of this oscillator is controlled by a phase locked loop circuit when the camera timing is "gen-locked" to external vertical and horizontal drive signals. The data rate in pixels per second is the master clock frequency divided by 2.

Timing waveforms for sensor drive and sync signals for the formation of NTSC compatible video are derived from the master clock signal. These timing signals are then fed to the drive board where the TTL level signals are altered to CCD drive level signals required to operate the sensor. From the drive board, sensor clocks are fed through the 31-pin D connector to the sense head and the composite sync signal is forwarded to the video processor board.

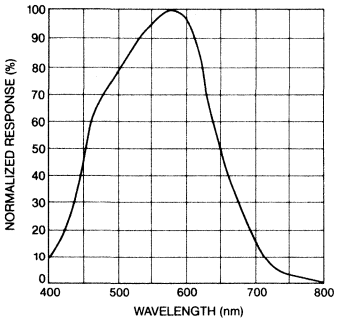
The video processor receives sensor video from the CCD in the sense head. The video is line clamped, amplified and blanked with composite blanking from the logic board, and may be summed with a composite sync signal from the drive board to yield RS170 composite video at the BNC output at the back of the camera. An Automatic Video Gain Control circuit may be actuated by connection of pin 18 to pin 19; about 20 db of gain increase is available.

Power Supply Unit

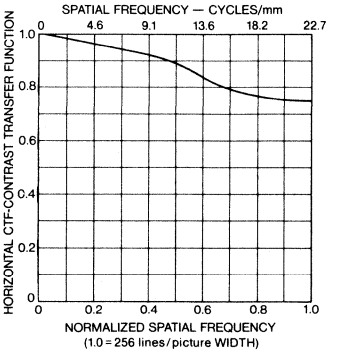
The cameras require inputs of ±15 and +5Vdc which are provided by the Power Supply Unit. Regulators on-board provide all voltage levels needed to drive the amplifiers and various clocks. The power supply unit voltages are derived from power line voltages of 120±10 or 240±20Vac, 47–63Hz. The front panel of the power supply unit provides BNC-connector access to composite blanking, composite sync, vertical drive and horizontal drive input and output signals and an external clock input as TTL levels. The rear panel contains connectors for interfacing the camera and power supply to the VIP100 Vision Interface Processor. A 6' (approx. 2m) cable is provided for interconnection of the camera control unit and the power supply.

TYPICAL PERFORMANCE CURVES

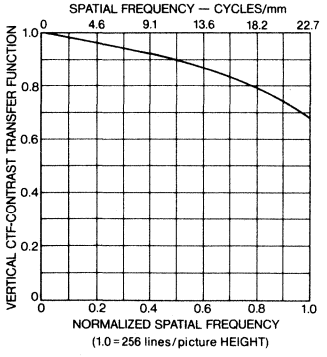
NORMALIZED SPECTRAL RESPONSE



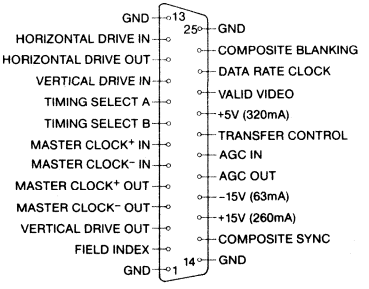
HORIZONTAL CONTRAST TRANSFER FUNCTION



VERTICAL CONTRAST TRANSFER FUNCTION



I/O PIN CONNECTIONS

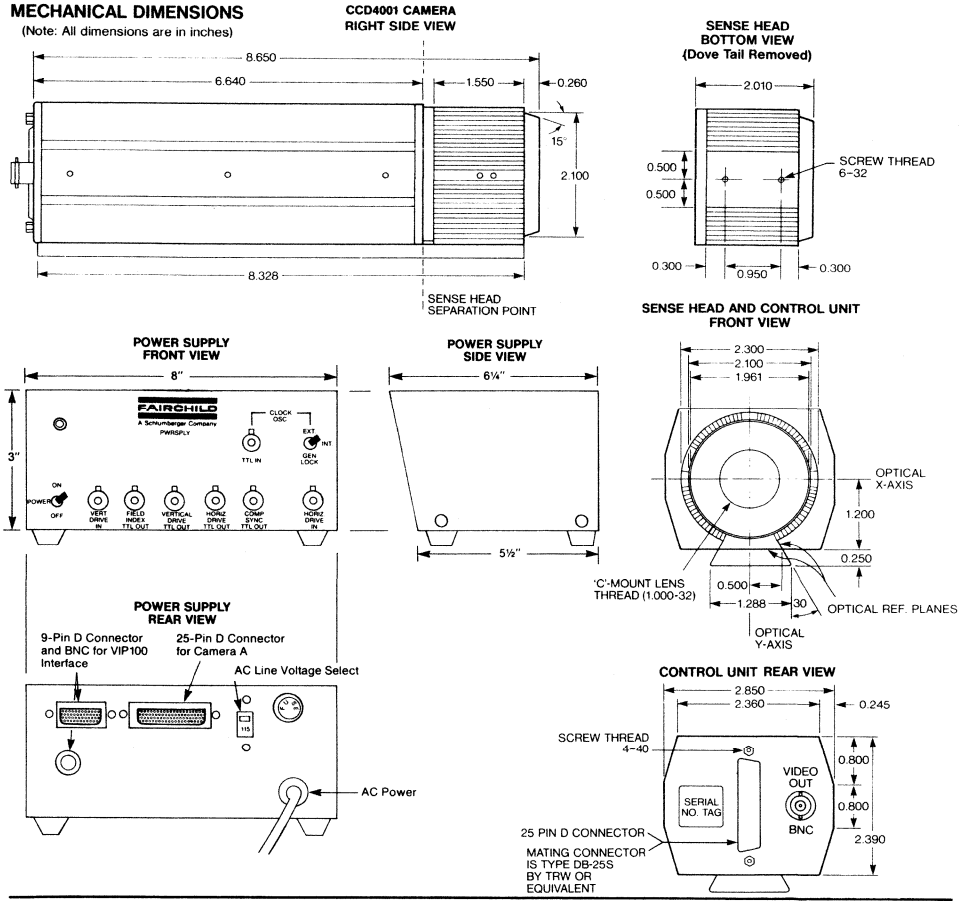


MATING CONNECTOR IS TYPE DB-25S
BY TRW OR EQUIVALENT

CCD4001

MECHANICAL DIMENSIONS

(Note: All dimensions are in inches)

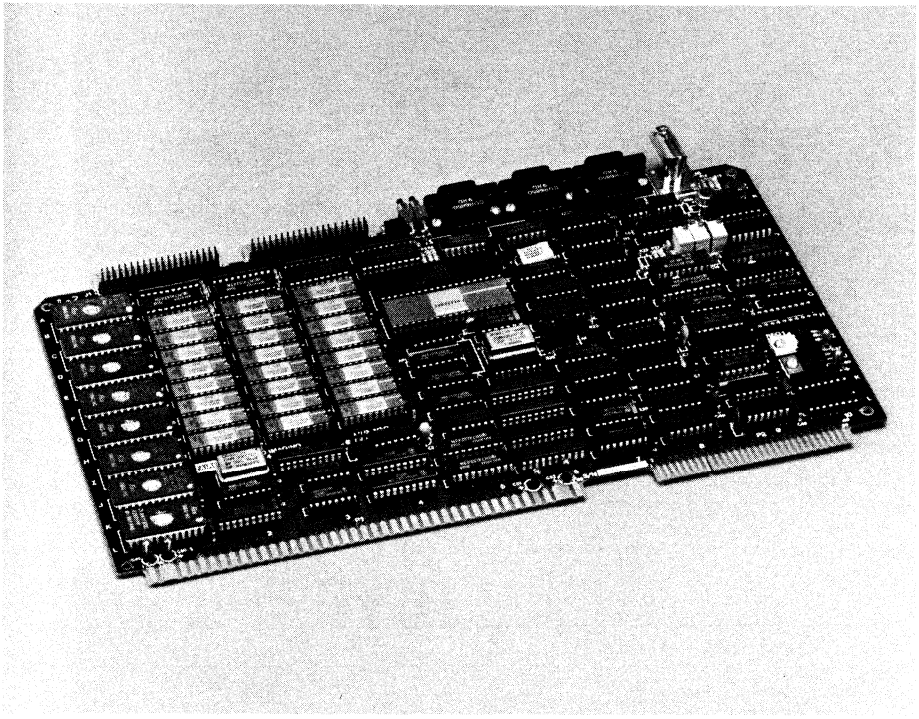


OPTIONS AND ORDER INFORMATION

Order Code	Description
CCD4001	Includes camera, power supply unit, interconnect cable and remote sense head cable.
CAM4001	CCD4001,less power supply unit, interconnect cable and sense head cable.
PWRSPLY	Power Supply Unit for CAM4001
CABL4001	Remote Sense Head Cable for CAM4001
Lenses	1" Vidicon type C-mount lenses are available in focal lengths of 13mm, 25mm and 50mm.
Monitor	NTSC monitor

FAIRCHILD
A Schlumberger Company

CCD



Vision Processing

VIP100
Vision Interface Processor

CCD Imaging

DESCRIPTION

The VIP100 is a versatile Multibus* formatted video processing card which can be used as a simple frame-grabbing memory for camera to computer interfacing or as a sophisticated stand-alone processor, capable of performing a host of industrial inspection and robotic vision functions such as:

- Non-Contact Measurement
- Defect, Surface Flaw and Edge Flaw Detection
- Automated Parts Sorting
- Optical Character Recognition
- Shape and Pattern Recognition
- Object Recognition
- Robot Guidance

Single-board processing is accomplished with use of an on-board high speed F9445 16-Bit Microprocessor in combination with an F9470 Console Controller. Under control of the F9445, converted digital data stored in the resident memory may be acquired through either the Multibus, a 16-Bit parallel port or either of two RS-232C ports.

The F9445 Microprocessor and F9470 Console Controller are supported by 24K words of static RAM plus space for 16K words of 2732 EPROM. Of the 16K words EPROM space, 8K words are utilized for storage of a powerful absolute assembly language (AAL) monitor program, our customized PEPBUG-45 and with Fairchild's optimized BASIC program, PEPBASIC-45, which is enhanced with vision primitives.

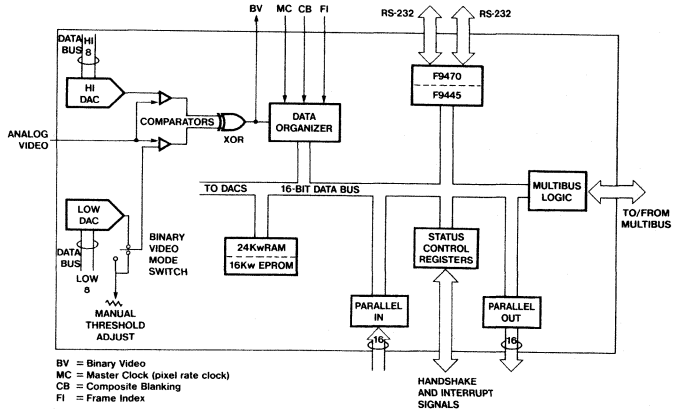
The VIP100 accepts either standard RS170 or non-standard video. Input anolog data is converted into binary (black-white) formats by comparison to two programmed DAC voltages. Binary video signals are exclusive ORed and packed on a pixel-by-pixel basis into 16-bit words for storage by the F9445. Once in memory, the video information is available for on-board processing, or transfer to a host processor.

* Multibus is a trademark of Intel Corporation.

FEATURES

- **REAL TIME CAMERA DATA ACQUISITION FROM NTSC OR NON-STANDARD VIDEO.**
- **COMPATIBLE WITH FAIRCHILD AUTOMATION AND LINE SCAN CAMERAS.**
- **STAND-ALONE COMPUTING CAPABILITY.**
- **IEEE 796 (MULTIBUS) COMPATIBLE: MASTER D16, M20, I16, V023EL.**
- **HIGH SPEED F9445 16-BIT MICROPROCESSOR.**
- **24K WORDS STATIC RAM, 16K WORDS EPROM CAPACITY.**
- **POWERFUL MINI-COMPUTER INSTRUCTION SET.**
- **ABSOLUTE ASSEMBLY LANGUAGE MONITOR, PEPBUG-45**
- **PEPBASIC-45 WITH VISION PRIMITIVES.**
- **TWO RS-232C I/O PORTS WITH VIRTUAL CONSOLE.**
- **SEPARATE USER CONFIGURABLE 16-BIT DATA INPUT AND OUTPUT PORTS.**
- **STATUS/CONTROL REGISTERS.**
- **1:1 PIXEL CONVERSION FROM AUTOMATION AND LINE SCAN CAMERA FAMILIES.**
- **BINARY OR TERTIARY VIDEO CONVERSION.**
- **PROGRAMMABLE BINARY THRESHOLDS.**

BLOCK DIAGRAM



VIP100

HARDWARE COMPONENTS

CPU — F9445. Fairchild's 16-Bit, high speed bipolar microprocessor utilizing Isoplanar Integrated Injection Logic (I^3L) technology. Typical instruction execution times are shown in the adjacent table.

Console Controller — F9470. Operates in two modes: virtual console control and I/O service. In console control, communication with the F9445 is controlled by the F9470. In I/O service mode, the F9470 acts as a serial I/O controller, interfacing the RS-232C I/O ports to the VIP100.

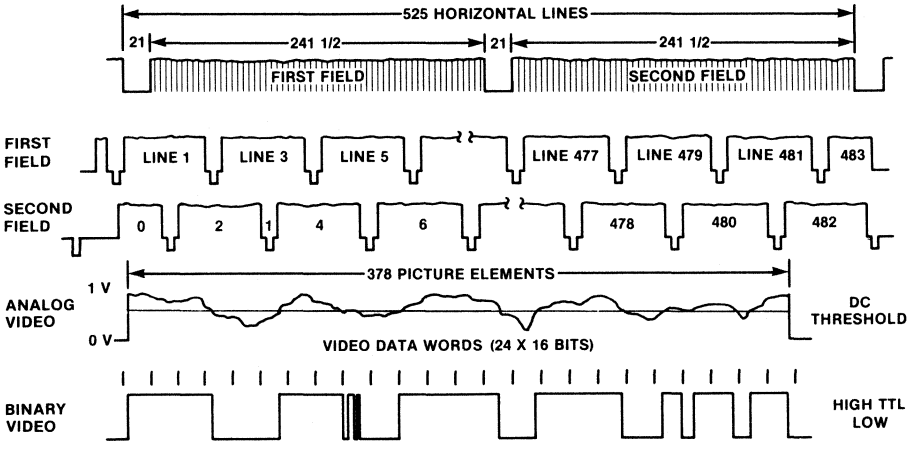
Video Converter — Composed of two 8-Bit DACs, two comparators, an XOR gate, a 16-Bit SIPO shift register. Thresholding of the DACs can be accomplished either under program control or manually through a binary video mode switch. The diagram below illustrates how the video converter groups the converted binary pixels into 24 16-Bit video words representing one video line from the CCD3000 camera.

F9445 INSTRUCTION EXECUTION TIMES*

Instruction	Clock Cycles	Execution Times in microseconds		
		16 MHz	20 MHz	24 MHz
COM	6	0.375	0.3	0.25
NEG	6	0.375	0.3	0.25
MOV	6	0.375	0.3	0.25
INC	6	0.375	0.3	0.25
ADC	6	0.375	0.3	0.25
SUB	6	0.375	0.3	0.25
ADD	6	0.375	0.3	0.25
AND	6	0.375	0.3	0.25
OR	6	0.375	0.3	0.25
MUL	70	4.375	3.5	2.9
DIV	86	5.375	4.3	3.6
JMP	6	0.375	0.3	0.25
JSR	6	0.375	0.3	0.25
ISZ	22	1.375	1.1	0.92
DSZ	22	1.375	1.1	0.92
LDA	12	0.75	0.6	0.5
STA	12	0.75	0.6	0.5

* Note: Instructions shown are an example of the F9445 instruction set. For further details, refer to the F9445 data sheet.

VIDEO CONVERSION OF IMAGE DATA FROM CCD3000 INTO BINARY WORDS

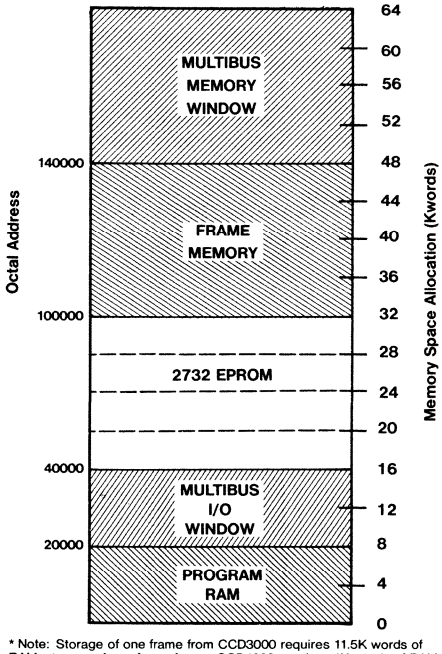


MEMORY (See Memory Map)*

RAM — 24K words static RAM.

EPROM — Eight sockets for 16K words of 2732 EPROM. Two sockets (one bank) are populated with 4K words containing the PEPBASIC-45 monitor program and two sockets are populated with vision-enhanced BASIC.

MEMORY MAP*



* Note: Storage of one frame from CCD3000 requires 11.5K words of RAM; storage of one frame from a CCD4000 requires 4K words of RAM. External memory may be expanded in any combination of RAM or ROM up to 1M bytes via the Multibus.

INPUTS/OUTPUTS

Analog Video In — Accepts 0–1 V P-P analog video or NTSC compatible RS170 composite video.

Camera Timing In — Requires a pixel rate clock (MC), blanking (CB), and a frame index signal (FI). These signals are available from Fairchild models CCD3000 and CCD4000 automation cameras.

Binary Video out — A latched TTL level binary video signal is available from the XOR gate in the video converter.

IEEE 796 (Multibus) I/O — Master D16, M20, I16, V023EL. Has multi-master capability.

Parallel I/O — Two-user configurable TTL-compatible 16-Bit I/O ports (one input, one output), with Status/Control Lines.

Serial I/O — Two programmable, asynchronous channels, with RS-232C interfaces. Each channel is software-selectable to rates of 110, 300, 1200, 1800, 2400 or 4800 baud.

BOARD PHYSICAL CHARACTERISTICS

Weight — 17 oz. (approximately)
Length — 12.0" (305 mm)
Height — 7.5" (191 mm)
Thickness — 0.75" (19 mm)

CONNECTORS

IEEE 796 (Multibus) — Composed of:
An 86-pin edge card connector with 0.156 inch center-to-center finger spacing. Edge connector is compatible with SAE M series edge board connectors or equivalent.
A 60-pin edge card connector with 0.100 inch center-to-center finger spacing. Edge connector is compatible with SAE 7000 Series edgeboard connector or equivalent.

Parallel I/O Ports — Two 40-pin edge card connectors with 0.100 inch center-to-center finger spacing. Edge connector is compatible with SAE 6700 Series edgeboard connectors or equivalent.

Serial I/O Ports (RS-232C) — Each is a 9-pin subminiature "D" right angle connector compatible with mating connector TRW DE-9P or equivalent.

Camera Timing In — A 9-pin subminiature "D" right angle connector compatible with mating connector TRW DE-9P or equivalent.

Analog Video In — Right angle BNC connector.

POWER REQUIREMENTS

+12V at 0.2A (typ)
−12V at 0.2A (typ)
+5V at 3.5A (typ)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature Range — 0° C to +50° C
Humidity — 0% to 90% (non-condensing)

SOFTWARE SUPPORT

PEPBUG-45 Monitor — The VIP100 is accompanied by a pair of EPROMS that contains our PEPBUG-45 Monitor program. This powerful debugging tool provides commands for trouble shooting assembly-language programs.

PEPBASIC-45 — The VIP100 is equipped with a pair of EPROMS containing a Fairchild mini BASIC enhanced by the addition of vision primitive commands and functions.

Development System — The VIP100 can be tied to another computer or a development system, such as the Fairchild System-1 (FS-1), for large program editing, assembling/compiling, and general file storage and handling. Cross-assembler software packages are available for creating machine-executable programs in formatted form.

Up-Load/Down-Load — The VIP100 is capable of up-loading or down-loading programs via one of the two RS-232C ports.

Modular Software — Fairchild is developing modular software packages for the VIP100. Please call the factory for the latest details.

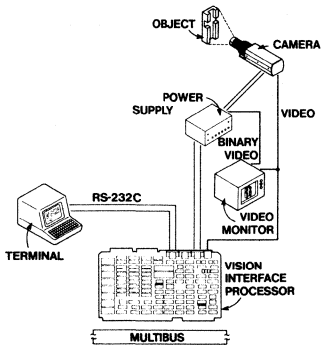
FAIRCHILD
A Schlumberger Company

CCD

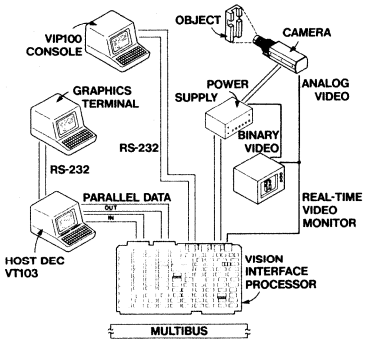
VIP100

POSSIBLE VIP100 SYSTEM CONFIGURATIONS

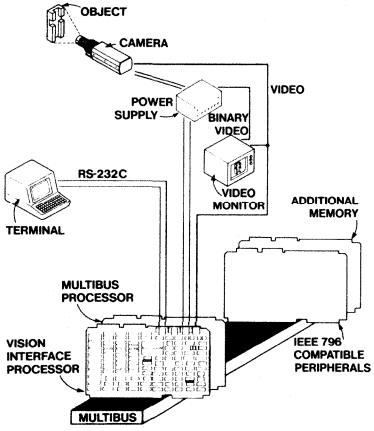
Single-Board System



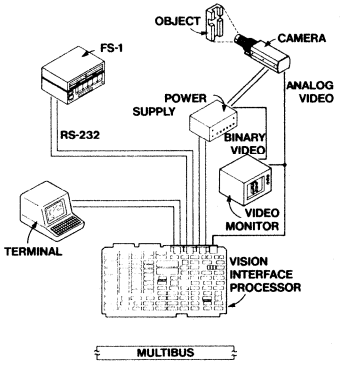
For Non-Multibus Host Interface



Multiprocessing



For Software Development



ORDER INFORMATION

To order the VIP100 Video Interface Processor, please use the appropriate ordering code from the table below:

Order Code	Description
VIP100-20	VIP100 with 20 MHz F9445

For further information on CCD products, call your nearest Fairchild sales office, representative or distributor. For engineering assistance call (415) 493-8001 (TWX 910-373-2110) or write Fairchild CCD Imaging, 3440 Hillview Ave., Palo Alto, CA 94304.

CCD FUNDAMENTALS

No math—just a straightforward explanation of how CCD memory units and video devices operate and what they can do for you!

By Frank H. Bower
Fairchild Camera and Instrument Corp.
Mountain View, California

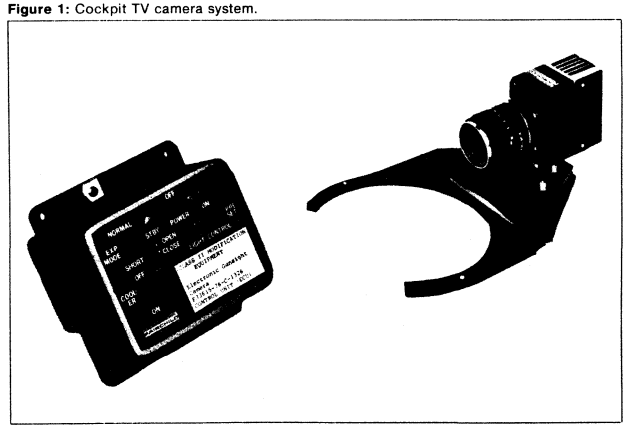
Charge-coupled devices (CCDs) are a new family of silicon semiconductor components capable of performing the general functions of image sensing, analog signal processing, and digital or analog memory. To realize the CCD concept's full capability, improved LSI techniques have been developed and basic NMOS processes substantially refined. Recognizing the technical advantages of using CCDs in defense systems, military and other government agencies started funding a number of research and development programs in the early seventies to accelerate the development of practical devices.

Today, there is a small but growing number of manufacturers offering high-performance CCD image sensing devices, analog signal processing devices, and large capacity digital memory integrated circuits. Several laboratories are also developing and building small numbers of special devices with government contractual support.

CCD Linear Imaging Devices (LIDs) have made possible the new generation of fast facsimile machines now reaching the market. They are also used in high speed mail sorting, rapid non-contact inspection and quality control measurement, and "smart" computer-controlled material handling systems. Real-time aerial mapping, reconnaissance, and surveillance systems have been improved by the application of high resolution LIDs as optical sensors.

CCD Area Imaging Devices (AIDs) are used in small, rugged, low power TV cameras capable of operation in very low light levels such as one-quarter moonlight. They have been applied in robots and automatic production systems as well as in miniature TV cameras for military systems (Figure 1).

Figure 1: Cockpit TV camera system.



The Charged-Coupled Device

The CCD operating principle is called "charge-coupling." Finite amounts of electrical charge called "packets" are created in specific locations in the silicon semiconductor material. Each specific location, called a

"storage element," is created by the field of a pair of gate electrodes very close to the surface of the silicon at that location. By placing the storage elements adjacent to each other, in a line for instance, voltages on the adjacent gate electrodes can be alternately raised and lowered and cause the individual charge packets beneath them to be passed from one storage element to the next (Figure 2). Since each charge packet may be of different size, the line of elements becomes a very simple analog shift register. All CCDs are basically shift registers, and because the transfer of charge from each storage element to the next adjacent element is very efficient, the amount of charge in each packet stays substantially the same, even after it has been passed from one element to as many as a thousand sequentially adjacent elements. Since the amount of charge in each packet is unique, the string of charge packets can represent analog information. The device is, in a sense, storing that information until it is delivered as an electrical signal from the charge detector built into the device at the end of the charge-coupled register.

This shift register performance is the basic characteristic of CCDs used in analog signal processing and memory devices. Figure 3 shows a diode-gate structure by which information is put into and taken out of the CCD register to allow operation in an electronic system operating with currents and voltages rather than with the charge-packets manipulated in the CCD itself.

Performing the image sensing function utilizes another basic characteristic of silicon semiconductor devices. This is the photoelectric effect by which free electrons are created in a region of silicon illuminated by photons in the approximate spectral range of 400 (blue) to 1100 (near infrared) nanometers wavelength. Response peaks at about 800 nanometers. Absorption of such incident radiation in the silicon generates a linearly proportional number of free electrons in the specific area illuminated. If a silicon device structure having a repetitive pattern of small but finite photo-sensing sites is created, the number of free

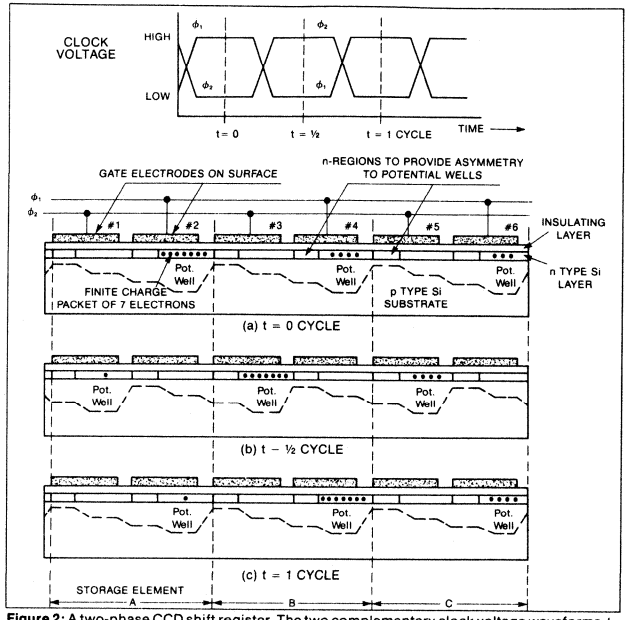


Figure 2: A two-phase CCD shift register. The two complementary clock voltage waveforms ϕ_1 and ϕ_2 are connected to alternate closely-spaced gate electrodes on the surface of the thin insulating layer on the silicon. A deep potential well which attracts electrons is created under the electrode clock voltage HIGH and disappears under the electrodes at clock voltage LOW. At t = 0, ϕ_2 voltage is HIGH and the finite charge packet of seven electrons is in the potential well under gate electrode #2 in storage element "A". At t = ½ cycle later, the potential well under gate #2 has collapsed due to ϕ_1 having gone LOW, and, since at the same time the adjacent electrode #3 connected to ϕ_2 has gone HIGH, the seven electron charge packet has been attracted to the new potential well under electrode #3. Another half cycle later, at t = 1 cycle, the potential well under electrode #3 has collapsed with ϕ_2 going LOW and the electron packet moves to the new well under electrode #4 which has gone HIGH with clock voltage ϕ_1.

Continued from page 17

electrons generated in each site (charge-packet) will be directly proportional to the incident radiation on that specific site. If the pattern of incident radiation intensity is a focused light image from an optical system viewing a scene, the charge-packets created in the finite photo-sites array will be a faithful reproduction of the scene projected on its surface.

After an appropriate exposure time, during which the incident light on each site is generating its time and intensity proportional electron charge-packet, the charge-packets are simultaneously transferred by charge-coupling under an adjacent single long gate-electrode, to a parallel CCD analog transport shift register. The single long gate is called the transfer-gate (Figure 4).

Each charge-packet corresponds to a picture element (pixel) and, when transferred to the adjacent CCD transport shift register, continues to faithfully represent the total sensed radiant energy which was absorbed in the specific photo site. The transfer gate is immediately returned to the non-transfer clock level (LOW) so photo-sites can begin integrating the next line of incident image information. At the same time, the CCD analog transport register, now loaded with a parallel-transferred line of picture information in the form of charge-packets from a line of sensor sites, is rapidly clocked to deliver the picture information, in serial format, to the device output circuitry.

The output circuitry consists of an output gate-diode structure and appropriate reset and buffering signal

amplifiers. The output terminal delivers a sequence of electrical pulses, the amplitude of each being directly proportional to the charge-packet size generated in the photo-site where the charge-packet originated. Sample-and-hold circuitry, either on-chip or in the video processing support circuitry delivers a line of video information.

Linear imaging devices (LIDs) sense and deliver information a line at a time; they are electronically scanned in one dimension and are often called line-scan devices.

Area imaging devices (AIDs) have an X-Y array of sense elements and sense an area image. They are built with both vertical and horizontal transfer gates and transport registers, and deliver an entire field of video information from each integration (exposure) period in the form of a series of lines of video signal.

CCD Characteristics

• Temperature: the CCD works best at low temperatures. It has no problem at −55°C and can perform at full capability to +70°C. Above 70°C, storage-related parameters degrade rapidly due to physical properties of semiconductor materials. All semiconductor materials continuously generate hole-electron pairs due to thermal energy, even at room temperature. If there is a finite packet of electrons representing information in a storage element, and thermally generated electrons add to that packet over a period of time, the packet will become larger and eventually will no longer accurately represent the original information.

In image sensors, which are very high dynamic range analog devices, it is often desirable to provide cooling for low light level applications to reduce thermal electron generation. Since image sensor devices are used as single units or as a matrix of two to six devices, and dissipate on the order of 50 mW or less, cooling is relatively simple. In CCD memory, long registers could be a problem, so the devices are designed with "refresh" cells at frequent intervals in the register. These sense-and-restore cells detect the "1" or "0" at the output end of a shift register section before enough thermal electrons can be added to cause misinterpretation of the data. Practical economic considerations, however, limit the temperature range for CCD memory to about +70°C. Because of the very low power dissipated in CCD memory, it is practical to consider providing cooling to achieve economical military electronic systems.

• Speed: the speed limitation of CCD devices is theoretically that of electron mobility in silicon and experimental devices operating in the gigahertz range has been reported. Since surface-state trapping in the silicon slows the net mobility of carriers near the surface, "buried channel" devices are faster than "surface channel" devices. The practical limitation to operating speed is caused by the edge-dependent charging current associated with delivering the clock voltages to the capacitances of the shift-register gate electrodes (C dv/dt current). The clock-driver circuitry also dissipates increased power with increasing frequency of operation. Desired operating speed is, therefore, a very strong design consideration in determining how much of the clock driving function should be put on-chip, thus increasing chip temperature, or left for the system designer to provide on the board.

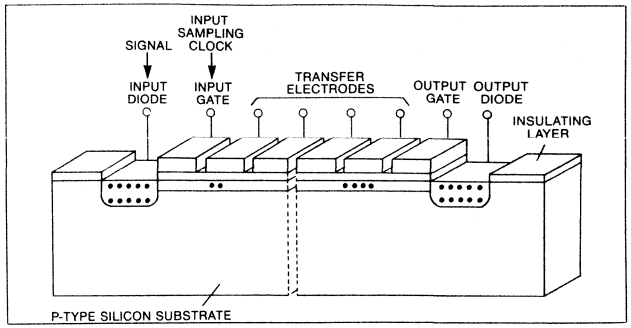


Figure 3: Input and output diode/gate structures for electrical input and output to a CCD shift register.

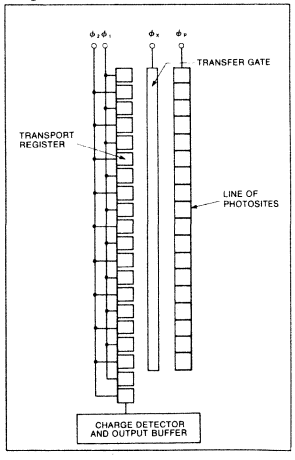


Figure 4: Simplified block layout of a linear image sensor.

• Reliability. Since materials used and the fabrication and packaging technology for CCDs are essentially those of NMOS LSI products, CCD device reliability equals that of NMOS. CCDs are inherently lower power devices and, therefore, the occurrence of thermally-induced failure mechanisms should be lower than that of NMOS. Manufacture of CCDs utilizes state-of-the-art NMOS production technology for its N channel, silicon gate, ion-implanted, surface passivated structure. Packaging can be in any of the commercial or high-reliability packages already proven in industry.

• Noise. The basic CCD register, heart of all CCD devices, is practically noiseless because it does not have PN junctions as do MOS and bipolar devices. Associated on-chip charge detectors and buffer amplifiers do have PN junctions and introduce some noise. Dynamic ranges of 10,000:1 have been achieved with cooling; 200:1 to 500:1 is common at room temperature.

• Radiation Hardness. CCDs are not basically "hard." They are fabricated on very lightly doped, high-resistivity silicon which has characteristics more easily altered by radiation than the more heavily doped silicon in bipolar and conventional MNOS devices. Buried channel CCDs have been reported to be more radiation tolerant than surface channel devices. Government sponsored development programs are under way at several laboratories to investigate methods for radiation hardening CCD devices.

• Packing Density. CCDs have a three to five times packing density advantage over the next most dense MOS large-scale-integrated circuits. This is primarily because the basic CCD storage element requires no electrical contacts. The storage and transport of the information in the CCD register are performed by the pattern of conductive gate electrodes on the surface of the thin oxide layer over the silicon. The gates require much less area per storage element than the combination of gates and ohmic contacts required for an MOS storage element. The 64 kilobit CCD memory device presently produced by Fairchild is a chip of silicon .175" × .230" in size.* With foreseeable improvements in LSI manufacturing technology and careful selection of the memory chip organization and on-chip peripheral circuits, devices with 256 kilobits capacity will be available within the next year or two.

CCD Applications in Miliary Electronics

Image Sensors. A CCD image sensor device can be configured as a line-scan device or as an X-Y TV type device. It can also be configured as a combination of the two basic structures for special applications. The line-scan device has a single line of sense elements and scans itself electronically in one axis—along the sense elements' centerline. It is often referred to as a Linear Imaging Device (LID). The X-Y device is an area matrix of sense elements capable of being electronically scanned in both X and Y axes to produce an area TV picture. It is often referred to as an Area Imaging Device (AID).

Most CCD image sensors have wide spectral range, and are nominally useful over the spectral range 450 to 1000 nanometers; i.e., visible through the middle of the near infrared regions. Standard commercial CCD image sensors will operate well up to a wavelength of about 800 to 900 nanometers; beyond that wavelength, they lose resolution rapidly. Resolution loss is due to the IR image photons generating electrons much deeper in the silicon and, therefore, beyond the attractive effect of the field created by the gate electrodes at the silicon surface. The generated electrons diffuse in the bulk of the silicon until they are either lost by recombination or move nearer to the surface where they are captured in the field of one of the sense elements. However, because of the time delay, they may arrive too late or in a sense element other than the one through which their exciting photon entered the silicon. The practical result is a loss of resolution or smearing of the image sensed. In some laboratories, work is being done to develop special CCDs for long wavelength IR image sensing.

All CCD image sensors consume low power and operate on low voltages. They do not exhibit lag or memory and are not damaged by intense light. Present devices will over-saturate and "bloom" under intense illumination but are not permanently damaged. Anti-blooming structures are under development.

Linear Imaging Devices(LIDs)

LIDs are configured as a single line of sensor elements on a long narrow chip. These devices are commercially available with 256, 1024, and 1728 elements with longer devices in development. LIDs are used in facsimile machines or spectrometers where the subject is a line pattern. When relative motion of the scene with respect to the sensor is provided by other means, the array can present a high-resolution TV-type picture. A continuous real-time picture can be obtained from a LID sensor in an aircraft or satellite passing over the surface of the earth at a constant altitude and velocity. Using a scanning mirror in the optical system can accomplish a similar result. LIDs applications include:

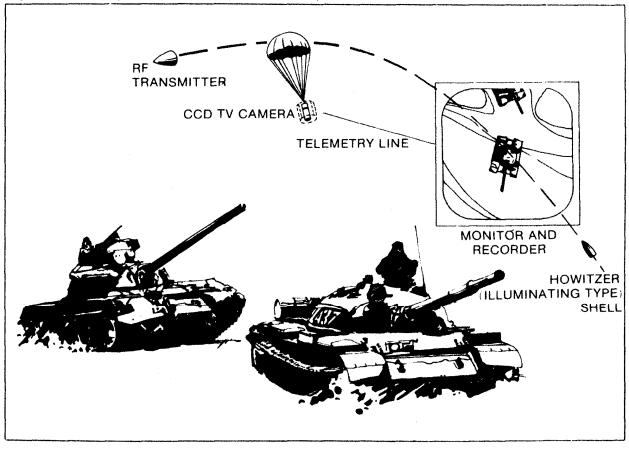
• High speed, high resolution facsimile (text, maps, fingerprints, photographs)
• Aerial mapping with high measuring accuracy
• Real-time reconnaissance and surveillance
• Bar-code reading
• Sorting parts, mail, currency, food
• Conveyorized product non-contact inspection
• Automatic warehouse routing and palletizing control

Special configurations of LID in which the array is eight to 64 elements wide (rather than one element wide) can be used for Moving Image Integration (MII) applications and are particularly effective in very low light level applications. Combined with analog delay lines, a LID can be used as the sensor for Moving Target Indication (MTI).

Area Imaging Devices (AIDs)

AIDs produce a TV picture. They are built in an array capable of being self-scanned in both the X and Y direction. These devices are available in 100 × 100 element and 244 × 190 element arrays; they have also been built in smaller sized arrays and in arrays of 400 × 400 and 488 × 380 elements. As an example of a commercially available device, the Fairchild CCD211 is a 244 × 190 element array with a sense area format equivalent to a Super 8 movie frame, and in a 3 × 4 aspect ratio for TV presentation. The device dissipates 100 mW when operated at a 7 MHz data rate, and operates at voltages of 12V to 15V. Its dynamic range is typically 300:1 at room temperature. Chip size is

Figure 5: Artillery launched TV system concept.



.245" × .245". AIDs applications include:

- Low light level search and surveillance
- Missile and RPV guidance
- Star tracking
- Remote or projectile TV reconnaissance (Figure 5)
- Cockpit or gunsight camera
- Space telescope

Large area AIDs are difficult to produce "blemish free" at low cost. Industry is aggressively addressing reduction and elimination of random defects to achieve practical, low-cost volume-producible AIDs with chip diagonal dimensions in the order of 0.500".

Analog Signal Processors

The CCD has been shown to be a nearly ideal analog shift register. The simplest analog signal processor is a variable analog delay line where the delay obtained is a direct function of the clocking frequency and the number of storage elements in the register. Differential phase and differential gain of 1% or less is available in commercial devices. Tapped CCD delay lines are excellent sampled analog filters and can be externally programmed to change filter characteristics, scan a frequency spectrum, or provide correlation of weak signals in a strong noise background. CCD Analog Signal Processor applications include:

- Video and audio variable delay lines
- Moving target indicator filter
- Signal correlation and convolution
- Sonic imaging
- Voice compression and scrambling
- Video frame-grabber
- Communications and secure communications filter
- Scan rate converter
- Spread spectrum filter

Digital Memory

All CCD memories are basically serial because of the fundamental shift register nature of charge-coupling. They are dynamic memories which require periodic refreshing and, like other semiconductor memories, they are volatile. While their latency is greater than bipolar and MOS memory, they are as much as fifty times faster than magnetic disc and drum memories. Because of the shift-register nature of CCD, the CCD memory devices are block-access oriented rather than random bit accessed. The high bit-count per package allows use of distributed memory and changes in computer architecture. CCD memory applications include:

- Cache memory
- Bulk storage
- Signal analysis for sonar, radar
- Synthetic aperture radar memory
- Digital delay
- Drum and disc replacement

As manufacturing technology continues to improve, all semiconductor memory will enjoy an increase in bit-density and a reduction in device and system costs due to the reduction in package count. CCD memory specifically will continue to remain more dense than bipolar and MOS memory for reasons previously stated. It is probable that CCD memory, because of its lower power dissipation, will be able to shift to packaging capable of being mounted more densely on P.C. boards. It is also probable that power dissipation can be reduced further by designing for operation at lower voltages. Peripheral circuitry such as on-chip drivers will be added to new CCD memory devices to the extent that added power dissipaiton can be tolerated and the additional silicon area required is economical from an overall systems cost standpoint.

Conclusion

Charge-coupled devices are now a family in production, bringing new capability to the military electronics systems designer. The high-volume, low cost production of area image sensors for TV sensing will require a combination of elimination of the causes of random defects from each step in the manufacturing process and improvement in the photo-lithographic techniques for patterning large area arrays so their area can be reduced without reducing responsivity.

Volume production of high performance analog signal processing devices such as filters requires definition of a volume market sufficient to warrant the development costs and application of resources. Increased control of manufacturing processes, particularly accuracy of the photo-lithographic process or its electron-beam successor, will allow the dimensional control necessary to produce devices which are linear over a large dynamic range and have the high rejection characteristics desired.

CCD memory will move ahead in the next few years to 256K bits per package from the present 64K level. Further, reduced power dissipation per bit and more compact packaging are probable. Ω

CHARGE-COUPLED DEVICES

The products of a new concept in semiconductor electronics, they hold considerable promise in applications as diverse as image sensors and information-storage elements for computer memories

by Gilbert F. Amelio

For the past four years there has been a growing excitement among solid-state physicists about a new concept in semiconductor electronics that may someday have an impact on our lives as dramatic as that of the transistor. The new concept is charge-coupling and its practical manifestation is the charge-coupled device.

Like the transistor, the charge-coupled device is a concept of semiconductor electronics; as such it is subject to the same physical laws that govern the transistor's dynamics and fabrication. That, however, is where the similarity ends. Although the charge-coupled device shares much the same technological base with its distinguished predecessor, it is a functional concept that focuses on the manipulation of information rather than an active concept that focuses on the modulation of electric currents. Transistor technology has made possible computer-memory components with thousands of memory elements on a single chip of silicon; charge-coupling is making possible comparably sized memory components with tens of thousands or even hundreds of thousands of memory cells per silicon chip at approximately the same cost.

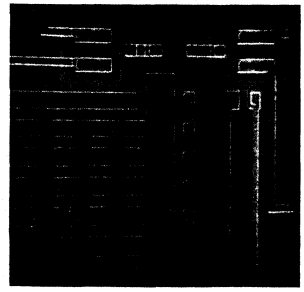
What is charge-coupling? It is the collective transfer of all the mobile electric charge stored within a semiconductor storage element to a similar, adjacent storage element by the external manipulation of voltages. The quantity of the stored charge in this mobile "packet" can vary widely, depending on the applied voltages and on the capacitance of the storage element. The amount of electric charge in each packet can represent information.

Perhaps the easiest way to visualize the operation of a charge-coupled device is through the use of a mechanical analogy. Imagine a machine consisting of a series of three reciprocating pistons with a crankshaft and connecting rods to drive them [*see top illustration on next two pages*]. On top of one or more of the pistons is a fluid. Note that rotating the crankshaft in a clockwise manner causes the fluid to move to the right, whereas rotating the crankshaft in a counterclockwise manner would cause the fluid to move to the left. Since it takes three pistons to repeat the pattern, this arrangement is called a three-phase system. If it is desired to move the fluid in one direction only, a two-phase system can be devised by imposing an asymmetry on the piston design [*see bottom illustration on next two pages*]. Regardless of the direction of rotation, the fluid now advances to the right.

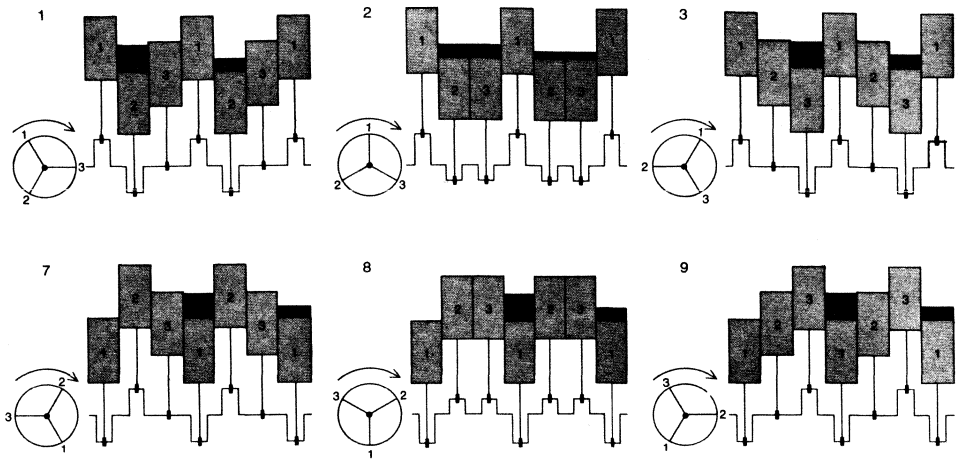
Analogous charge-coupled devices can be fabricated of silicon [*see illustrations on page 26*]. The devices consist of a "*p* type" silicon substrate (in which electrons are normally the signal carriers) with a silicon dioxide insulating layer on its surface. An array of conducting electrodes is deposited in turn on the surface of the insulator. The electrodes can be interconnected to establish either two-phase or three-phase operation. Underlying the insulator and within the bulk of the semiconductor the electrical conductivity of the silicon can be selectively altered to form "*n* type" material (in which not electrons but electron "holes" are normally the signal carriers). The correspondence with the machine in the mechanical analogy is realized by supposing that the fluid represents an accumulation of electrons, that the pistons represent the potential energy associated with the voltages applied to the electrodes and that the crankshaft and connecting rods represent the driving voltages and their relative timing.

When a periodic wave form called a "clock" voltage is applied to the electrodes, some of the electrons in the vicinity of each electrode will form a discrete packet of charge and move one charge-coupled element, or unit cell, to the right for each full clock cycle. The packets of electron charge therefore move to the right as a result of the continuous lateral displacement of the local "potential well" in which they find themselves. They are thus—or so it seems—always falling.

The creation of the necessary potential well in the semiconductor substrate deserves some elaboration because of its central importance to the charge-coupling concept. In this context a potential well is a localized volume in the silicon that is attractive to electrons; in other words, it is the most positive place around and hence is a desirable location from the point of view of the negative electron. Potential wells are formed in a charge-coupled storage element by the interaction of the different conductivity-



CLOSEUP VIEW of a small portion near the output of a charge-coupled photosensor array is provided by this scanning electron micrograph. Each element and its associated readout electrode measure 1.9 square mils.



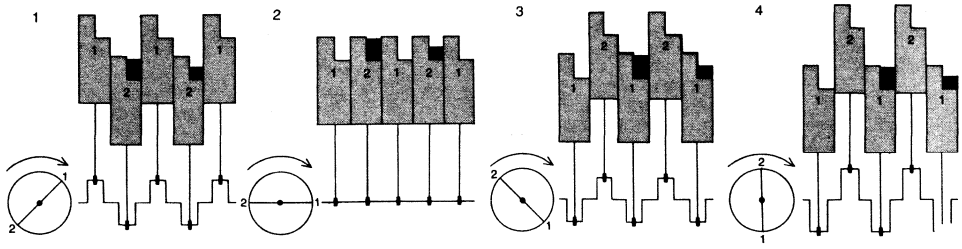
MECHANICAL ANALOGY useful in visualizing the operation of a charge-coupled device is depicted in this sequence of idealized drawings. The machine illustrated consists of a repeating series of three reciprocating pistons with a crankshaft and connecting rods to drive them. On top of one or more of the pistons is a fluid (*color*). Rotating the crankshaft in a clockwise manner, as shown

type regions of the silicon [*see illustration on page 27*]. This interaction forms a well for electrons such that the higher the clock voltage, the deeper the well. Any electrons in the well will move with the clock voltages.

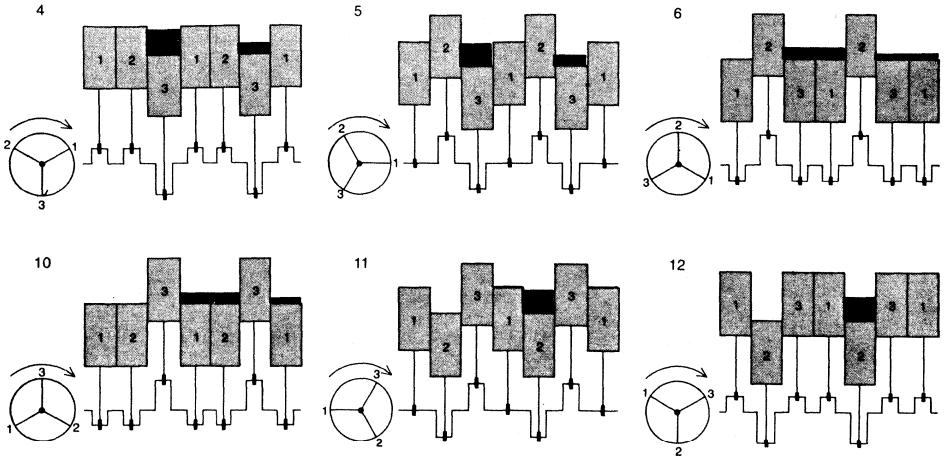
Now, if two or more wells of different depths are placed close to one another, the wells will overlap and charge may be "coupled," or transferred, from one storage element to the next as the depth of the well is altered by the clock voltages. Thus the external clock voltages on the electrodes cause the electrons to move in packets through the semiconductor in a potential-energy trough known as a channel. This mode of electron transfer is the essence of charge-coupling.

The phenomenon of charge-coupling is in itself inadequate for the purpose of constructing a useful device. A practical charge-coupled device must be able to introduce the necessary electrons into the structure and also have a means at some location in the channel for detecting the amount of charge in a packet. Thus for a structure to be classified as a charge-coupled device it must possess at least three attributes: input, charge-coupling and output.

As an example of a simple yet functionally complete charge-coupled device, consider a "shift register" consisting of eight three-phase elements, an input diode and gate and an output diode and gate [*see illustration on page 28*]. This structure is in fact very similar to the first charge-coupled device ever fabricated. The signal that is to be entered into the charge-coupled device is connected to the input diode, which acts as a source of electrons. If the input gate is held at a low voltage, no signal electrons can enter the channel. In order to put a packet of electrons into the device it is necessary to wait until the first-phase electrodes are in the high-voltage condition and then "turn on" the input gate by raising its voltage. Electrons fill the potential well until the energy level for electrons in the well is the same as that for the electrons in the source. The input-gate voltage is now lowered to isolate the source, and the charge packet created is ready for transfer down the channel. In the detection of the signal



ASYMMETRICAL PISTONS are added to the mechanical analogue in order to introduce the operating principle of a two-phase system. Regardless of the direction in which the crankshaft is rotated, the fluid now advances to the right. In the correspondence



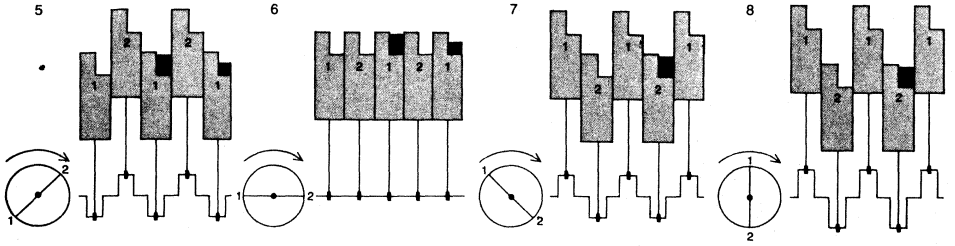
in this instance, causes the fluid to move to the right. If the crankshaft were to be rotated in a counterclockwise manner, on the other hand, the fluid would move to the left. This particular type of arrangement, which requires three pistons to repeat the pattern, is called a three-phase system. An analogous charge-coupled device can be fabricated of silicon (*see top illustration on next page*).

the charge is merely transferred to a "drain," or output diode, where it appears as a current in some external circuit. This simple charge-coupled device fulfills the function of an eight-bit shift register, a device potentially useful in computer architecture.

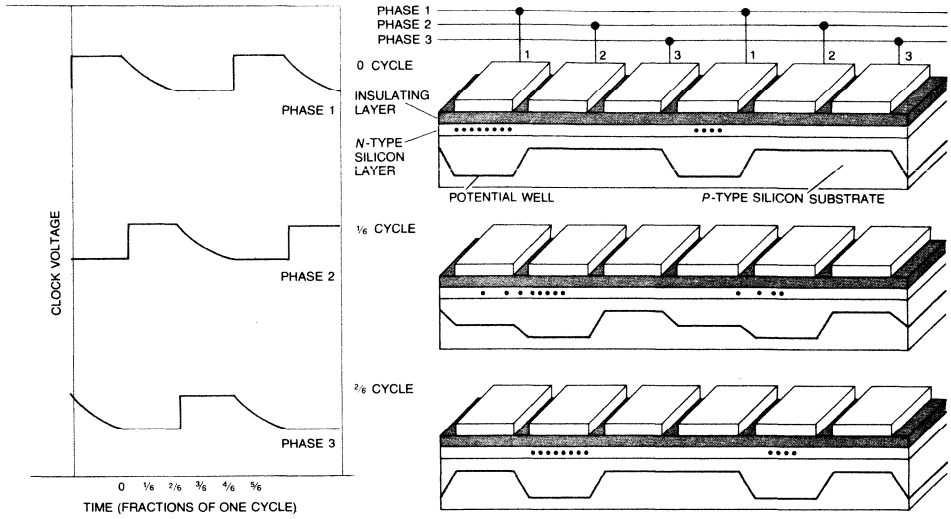
Devices fabricated and operated in this manner verify the predicted performance with one exception. Unfortunately not all the electrons advance with the packet on each transfer, and the residual charge appears in a trailing packet. The magnitude of such "charge-transfer inefficiency" is a function of the design of the device and the frequency of operation. Transfer inefficiency imposes a fundamental limitation on the speed and number of transfers for a practical charge-coupled device because of the resulting attenuation of the charge packet as it is moved through the device from one region to the next.

There are two reasons for charge-transfer inefficiency. First, the electrons may be inhibited from moving because of local regions of lower potential energy (corresponding to dents or ridges in the top of the piston in the mechanical analogy). Second, the frequency of operation may be so high that there is not enough time for all the electrons to follow the moving potential wells. The former problem is one that is influenced predominantly by the design details of the particular charge-coupled device. Researchers working on the development of such devices are continuing to explore this aspect of charge-coupling. Recent advances in technology have significantly reduced the seriousness of the problem. The problem of the speed of the electrons' motion, however, has more basic origins and deserves additional comment.

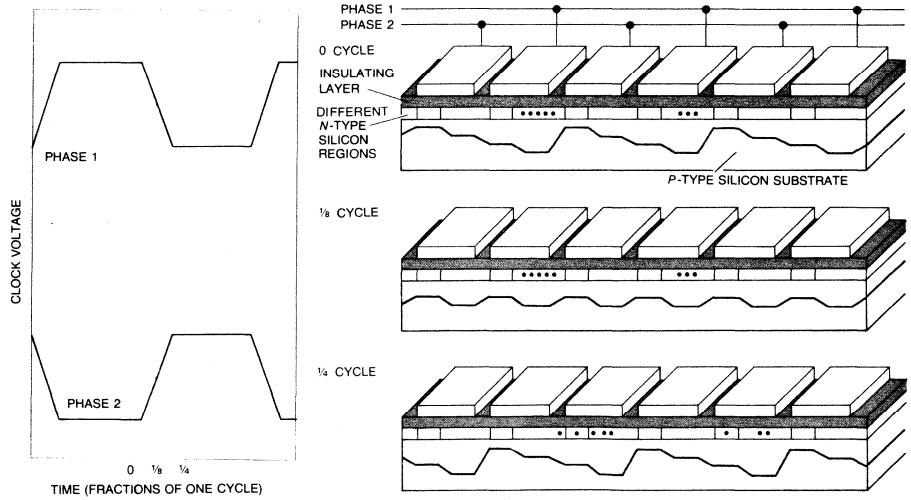
The electrons are induced to move to an adjacent region of lower energy (that is, a deeper potential well) by a combination of three influences: self-induced forces, field-aided forces and thermal forces. Self-induced movement results from the simple fact that a high-density packet of electrons (or any similar particles) tends to spread rapidly if the constraining force is removed, as is the case when the clock voltages change. This type of force is important during the



with an actual charge-coupled device the fluid represents an accumulation of electrons, the pistons represent the potential energy associated with the applied voltages and the crankshaft and the connecting rods represent the driving voltages and their timing.



TWO THREE-PHASE CHARGE-COUPLED ELEMENTS are shown in the cross-sectional diagram at right; the curves at left give the relative timing of the "clock voltage" wave forms for three-phase operation. The device consists of a "*p* type" silicon substrate (in which electrons are normally the signal carriers) with a silicon dioxide insulating layer on its surface. Conducting electrodes are deposited on the surface of the insulator. Underlying the insulator and within the bulk of the semiconductor the electrical conductivity of the silicon can be altered to form an "*n* type" layer (in which electron "holes" are normally the signal carriers). When the clock voltage is applied to the electrodes, some of the electrons in the vicinity of each electrode will form a discrete packet of charge (*black dots*) and move one element to the right for each full clock cycle. In effect the packets of electron charge move to the right as a result of the continuous lateral displacement of the local "potential well" in which they find themselves (*white contours in substrate*).



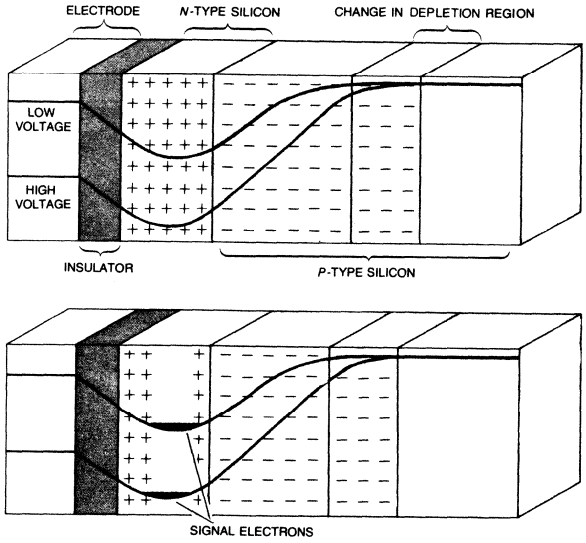
THREE TWO-PHASE CHARGE-COUPLED ELEMENTS are shown in these cross-sectional diagrams; again the curves give the relative timing of the clock voltages, this time for two-phase operation. Here the potential wells are given the required asymmetry by the introduction of different *n*-type conductivity regions just under the insulating layer. As in the illustration at the top, the external clock voltages on the electrodes cause the electrons to move in packets through the *n*-type semiconductor layer toward the right.

early stages of charge transfer. Field-aided movement is important if the structure is designed in such a way that electric fields exist to assist the electrons' motion in the desired direction. This corresponds to adding a slope to the top of the pistons in the mechanical analogy. If such a force is present, it is important only toward the end of the charge-transfer cycle. Thermal forces arise from the fact that the electrons receive thermal energy from the silicon lattice and as a result are free to move about randomly. In their random motion they tend to move to regions of minimum electron energy. This type of force is important at the end of the transfer cycle only if field-aided forces are absent.

The self-induced force lasts for only a brief time at the beginning of the transfer cycle, but it is responsible for moving about 90 percent of a "saturation," or full, charge. If the field-aided force is present, it is responsible for moving most of the remaining charge at a rate directly proportional to the strength of the electric field and inversely proportional to the distance between the electrodes. If the field-aided force is not present, the remaining charge will move under the influence of thermal forces at a rate directly proportional to the temperature and inversely proportional to the square of the distance between the electrodes. This rate is usually lower than that resulting from the field-aided force, although at small dimensions it becomes increasingly significant because of its inverse quadratic dependence on distance.

Although these forces are responsible for moving only a comparatively small fraction of the total charge packet, they are important because very little transfer inefficiency can be tolerated in practical devices. For example, if 1 percent of the charge is left behind at each transfer, most of a charge packet will have dispersed after only 100 transfers. In general the charge-transfer inefficiency must approach one part in 10,000 to be considered acceptable for most practical applications. In spite of this requirement, devices that can be operated at frequencies of up to 100 megahertz (100 million cycles per second) are possible if the structures are made small enough. With modern microelectronic manufacturing techniques it is possible to design and build a charge-coupled unit cell with dimensions of less than a mil (a thousandth of an inch) on a side, although it is not always appropriate to do so.

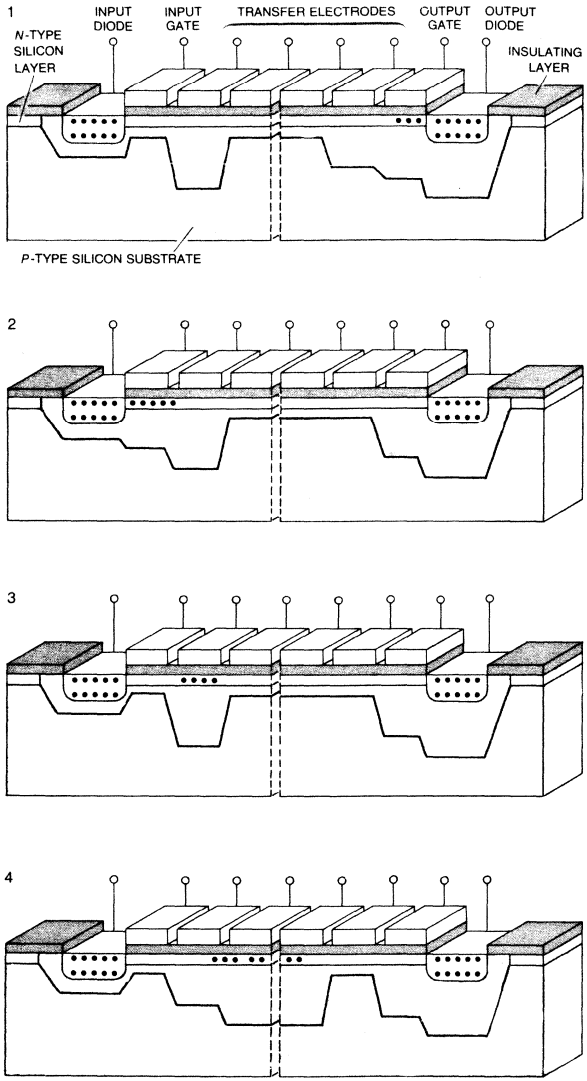
Unit cells of such small dimensions are possible because of the simple nature of the charge-coupled structure, which does not require direct contact with the silicon in the array region. This arrangement is to be contrasted with conventional transistor technology, which in general requires several contacts per functional cell. Contacts consume a significant amount of valuable silicon because of the contact area and the tolerances needed to form a good electrical connection. From the manufacturing viewpoint it is this feature more than any other that makes charge-coupled devices so attractive.



POTENTIAL-ENERGY PROFILES for a typical charge-coupled information-storage element are shown here as a function of distance into the bulk of the semiconductor at right angles to its surface. (In order to show the potential wells clearly, this diagram has been rotated by 90 degrees with respect to the preceding ones.) The charge-distribution patterns are shown for two situations: with no electrons in the well (*top*) and with some electrons in the well (*bottom*). As the curves indicate, the higher the clock voltage, the deeper the well.

The ability to generate, move about and detect many separate packets of electrons in a small piece of semiconductor material suggests that the charge-coupling principle can be applied to fulfill a number of information-processing requirements. In particular the highly ordered manipulation of charge packets characteristic of the operation of charge-coupled devices favors uses such as image sensing, computer-memory operation and sampled-signal processing. In each case the function is achieved by a proper combination of charge-coupled unit cells that operate individually exactly as described above.

Silicon, the semiconductor material of which charge-coupled devices are generally fabricated, is highly sensitive to visible and near-infrared radiation [*see illustration on page 9*]. In other words, when light falls on a silicon substrate, the radiation is absorbed (by means of the Einstein photoelectric effect), which results in the generation of electrons in a quantity proportional to the amount of incident light. If there is present an array of potential wells such as the one formed by charge-coupled devices, these electrons will fill the wells to a level corresponding to the amount of light in their vicinity. This "electro-optic" creation of electrons represents an input to the charge-coupled device that is entirely different from the input method required for the shift register discussed above and makes the charge-coupling concept useful for very different kinds of application. Nonetheless, the packets of electrons generated by the light can be moved, just as in the shift register, to a point of detection and converted to an electrical signal representative of the optical image incident on the device. That signal, after some conditioning, can be displayed on a cathode ray tube. In this way a charge-coupled device can



INPUT AND OUTPUT OPERATIONS of a simple eight-element, three-phase charge-coupled "shift register" are summarized in this series of diagrams. The signal enters the device by way of an input diode, which acts as a source of electrons. If the input gate is held at a low voltage, no signal electrons can enter the potential-energy "channel" (*1*). In order to put electrons into the device one must wait until the first-phase electrodes are in the high-voltage condition and then "turn on" the input gate by raising its voltage (*2*). Electrons fill the potential well until the energy level for the electrons in the well is the same as that for the electrons in the source. The input-gate voltage is now lowered to isolate the source (*3*), and the charge packet created is ready for transfer down the channel (*4*). The signal is detected by transferring the charge packet to an output diode, where it appears as a current.

become the heart of a television camera.

One of the significant advantages of charge-coupled image sensors over vacuum-tube sensors is the precise knowledge of the photosensor locations with respect to one another. In a camera tube the video image is "read" from a photosensitive material by a scanning electron beam. The position of the beam is never precisely known because of the uncertainty in the sweep circuits resulting from random electrical noise. In a charge-coupled sensor the location of the individual photosensor sites is known exactly, since it is determined during the manufacture of the component. Such "metric" accuracy is important for proper alignment in color cameras and in applications requiring data reduction of the acquired image (as in photographic missions in space and photogrammetry).

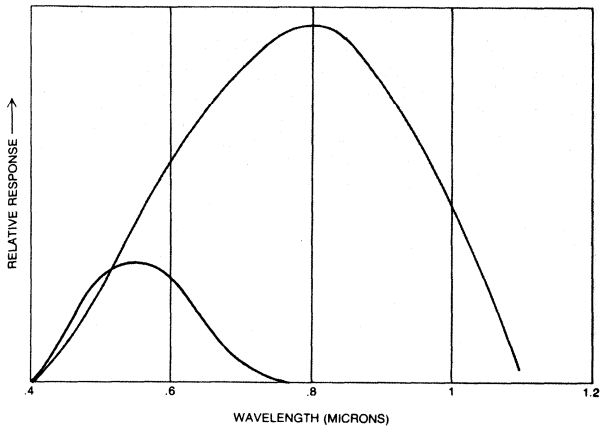
It is generally convenient for purposes of discussion to separate charge-coupled sensors into two categories: linear sensors and area sensors. A linear image sensor is a simple straight-line array of photosensors with the associated readout and sensing circuitry. An area image sensor is a two-dimensional mosaic of photosensors, again with the associated readout and sensing circuitry.

Linear image sensors are used for a host of applications, including air-to-ground and space-to-ground imaging, facsimile recording and slow-scan television. The image to be viewed is obtained by providing relative motion between the sensor and the scene with the axis of the array perpendicular to the direction of the motion. A resolution of 500 or more photosensor elements is usually required. A primitive linear imaging device can consist of nothing more than a charge-coupled shift register and an output diode. In this structure the image is acquired when one holds the potential wells stationary by stopping the voltage clocks for some period of time (the "integration time") and then rapidly reads out the information by starting the clocks. Such a simple charge-coupled device should be practical only in special applications that allow very long integration times. The reason for this limitation is the "smearing" of the image that results when the shift register is clocked at the same time that it is illuminated.

A really practical charge-coupled linear image sensor is more complex. It consists of a photosensor array for accumulating the photocharge pattern plus an associated charge-coupled shift register with one charge-coupled element for each photosensor element in order to move the resulting charge packets to an output point. The elements of the photo-

sensor array are individual charge-coupled storage elements with a common electrode called a photogate. They are electrically separated from one another by a highly concentrated *p*-type region called a channel stop. The photosensor array is separated from the charge-coupled shift register by a region over which there is an electrode called the transfer gate.

In operation the photogate voltage is held high and the charge generated by the incident radiation (the photocharge) is collected by the individual photosensor elements. At the end of the integration time the transfer-gate voltage is raised from its normally low voltage condition. The charge-coupled shift-register electrodes adjacent to the photosensor elements are also brought to a high-voltage state. The photogate voltage is then lowered and the accumulated photocharge transfers to the shift register. After that is accomplished the transfer-gate voltage is lowered and the photogate voltage is brought back to its normally high state for another integration period. Meanwhile the charge-coupled shift register is clocked for the purpose of reading out the charge pattern.



RELATIVE SPECTRAL RESPONSES of a charge-coupled silicon photosensor element (*colored curve*) and the human eye (*black curve*) are compared. The semiconductor material absorbs not only visible light (.4 to .7 micron) but also near-infrared radiation (.7 micron to 1.1 microns). The absorption of such radiation by a silicon substrate results in the generation of electrons in a quantity proportional to the amount of incident radiation. It is this "electro-optic" property that enables charge-coupled devices to be used as image sensors.

A high-density image sensor is more economically designed with one shift register on each side of the photosensor array. Since there must be one charge-coupled element for each photosensor element, the distance between photosensor elements is equal to the distance between the shift-register electrodes for a two-phase charge-coupled shift register and is equal to 1.5 times the distance between shift-register electrodes for a three-phase charge-coupled shift register. In this example the signal charge from the two three-phase shift registers is transported to a three-phase, two-element register for delivery to the on-chip preamplifier. If two-phase technology is used, however, it is possible to shift the charge directly into an output diode, which is in turn the input to the on-chip preamplifier. Note that in either case the information-output rate of the device is twice the rate of either of the long shift registers. It is clear from this example that a two-phase charge-coupled structure not only is easier to clock but also is more economical to lay out for a practical device. Even though it is somewhat more difficult to manufacture because of the required asymmetry, it is likely to dominate future designs of charge-coupled devices when fully developed.

A linear image sensor can be made to produce conventional two-dimensional images [*see illustration on next page*]. The image to be sensed is placed on a rotating drum, which provides the necessary motion of the image with respect to the device. The speed of rotation is synchronized with the vertical scan of the monitor. The charge-coupled linear image sensor provides each horizontal video line for the monitor by a complete sensing and readout operation repeated rapidly to supply all the horizontal lines for a full frame. In many applications the device is the moving element in the system, as in aerial reconnaissance, where the device is located in an airplane or a satellite.

The quality of image reproduction achievable with a linear charge-coupled sensor is excellent, reflecting the large dynamic range of the image sensor [*see illustration on page 31*]. The dynamic range is the ratio of the maximum to the minimum detectable image intensity. The quality of the reproduction demonstrates the very high transfer efficiencies and low electrical noise levels that can be achieved in existing charge-coupled devices.

Area image sensors are useful primarily for television-type camera applications. The image is obtained by conventional line-by-line scanning of the array mosaic and reproduction of the resulting video signal on a standard raster-scanned cathode-ray-tube monitor. A charge-coupled area image sensor designed for such a readout mode can be designed in a manner analogous to the linear image sensor. As in standard broadcast television, the image is read out in two separate fields by first reading all the even-numbered photosensor elements in each column and then all the odd-numbered photosensor elements in each column rather than by reading the odd and even elements in parallel, as in the case of the linear image sensor.

The area image sensor operates as follows. Light falling continuously on the photosensor sites produces electrons, which accumulate as charge packets in the potential wells created by the photogate voltage. After an interval of a thirtieth of a second the charge packets collected in the photosensors adjacent to all the phase-1 electrodes are transferred to the region under the phase-1 electrodes by raising the phase-1 voltage and lowering the photogate voltage. The charge packets in photosensor sites adjacent to the phase-2 electrodes do not transfer because the phase-2 voltage remains low. After the phase-1 transfer takes place the photogate voltage again goes to its normally high state and more electrons begin to accumulate in the depleted photosensor sites. The charge packets in the opaqued shift register are now transferred to the horizontal shift register at the top of the array. Each vertical transfer fills the horizontal register, which is then read out completely, producing a line of video information at the out-

put. After all these lines are read out (a procedure that takes only a sixtieth of a second) the photosensors adjacent to all the phase-2 electrodes are read out, and in a similar manner this second field is delivered as a video signal at the output. Finally, the entire operation begins again and is completed at regular intervals of a thirtieth of a second.

A typical image sensor designed to operate in this fashion consists of a rectangular 100-by-100 photosensor grid [*see illustration on page 22*]. Each photosensor element and associated readout electrode occupies only 1.9 square mils. All 10,000 elements fit on a chip that measures .12 by .16 inch. An image taken with a camera system using such a device can be displayed on a television monitor.

This image-sensing device and others made by charge-coupled techniques are still somewhat primitive, but they clearly point the way toward a powerful camera technology. The combination of solid-state reliability, low-voltage operation, low power dissipation, large dynamic range, metric reproducibility and visible and near-infrared response offers to the potential user a compelling advantage over vacuum-tube image sensors and other solid-state image sensors.

The charge-coupling concept is basically one of semiconductor electronics rather than one of electro-optics. Because of the electro-optic characteristics of silicon, however, the light-sensing properties of charge-coupled arrays have tended to dominate this new technology. Nonetheless, the data-handling properties of such arrays may be of equal or even greater significance.

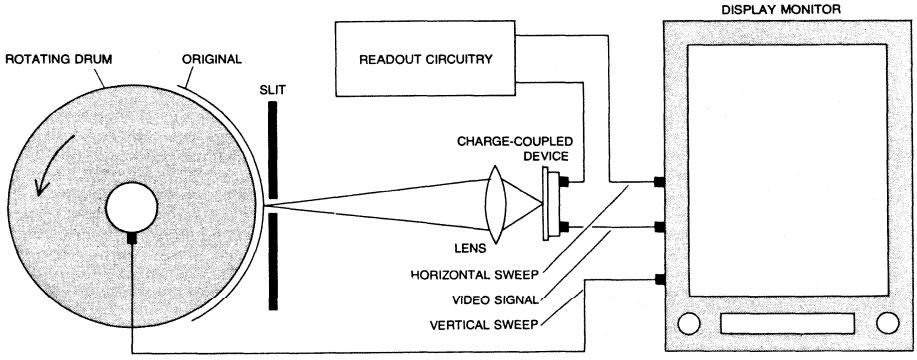
A charge-coupled semiconductor array is virtually ideal as a time-sampled analogue shift register. From the viewpoint of the electrical engineer this means a delay line where the delay is proportional to the readin/readout rate; if the array is long enough to contain the complete message, the readin and readout rates can be different and the maximum delay available is limited only by the thermal generation of random electrons. At low temperatures several minutes of delay are possible.

As a memory or digital-storage device, charge-coupled arrays can perform the functions of sequential access or hybrid tasks such as drum or disk storage. The use of solid-state charge-coupled arrays to eliminate all mechanical motion and parts is a strong advantage of a memory consisting of charge-coupled devices.

The intrinsic analogue nature of the charge packet in a charge-coupled device suggests broad potential for application to sampled-signal processing. In a fundamental sense the use of charge-coupled devices as image sensors is merely a special application of the device as an analogue shift register. If one restricts the definition of sampled-signal devices to those with an electrical (rather than an optical) input, then the predominant members of this class are variable delay lines and filters.

A delay line is a circuit that reproduces as accurately as possible an input signal delayed by a finite period of time. A delay line is "variable" if the time delay can be altered electrically. The charge-coupled device acts as a natural delay line since any signal placed on its input diode will appear at its output in sampled form after the interval required for the charge packets to be shifted through all the elements of the structure. The charge-coupled device can be used as a delay line in several ways. First, in the simple continuous mode the delay is equal to the number of unit cells divided by the frequency at which the device is clocked. Alternatively, whenever data appear in bursts, the charge-coupled shift register can be loaded with these data during the burst and the data retained for the desired interval and then read out. In this way the charge-coupled device is said to perform a "buffer" function.

A charge-coupled delay line offers major advantages over the more conventional glass delay line and even significant advantages over the more exotic acoustic-surface-wave devices [see "Acoustic Surface Waves," by Gordon S. Kino and John Shaw; SCIENTIFIC AMERICAN, October, 1972]. Among these are wide dynamic range (better than 60 decibels after 30 milliseconds at room temperature) and separate electronic control of propagation velocity and delay time. Delay lines with such flexibility will be of great value in communications and television applications and will simplify existing methods of producing controlled signal delays. One special application of significant interest is a "scan-rate converter" often required in video communications. Here the charge-coupled device operates in the buffer mode described above to accept and then read



TWO-DIMENSIONAL IMAGES can be reproduced with the aid of a linear charge-coupled image sensor in a variety of ways, one of which is outlined in this schematic diagram. The image to be sensed is placed on a rotating drum (*left*) whose speed of rotation is synchronized with the vertical scan of a conventional television display monitor (*right*). The charge-coupled device and the associated readout circuitry produce horizontal video lines at a rate rapid enough to build up a full-frame image on the screen of the monitor.

EXCELLENT REPRODUCTION obtained with a 500-element linear charge-coupled image sensor under widely varying light conditions is evident in these photographs. An apparatus similar to the one in the illustration on the opposite page was employed to scan the image. The photograph at left shows the original image to be scanned. The photograph at center shows the video display obtained from the charge-coupled system under optimum lighting conditions (30 foot-candles of illumination). The photograph at right shows the video display obtained from the same system but with the light level reduced 1,000 times; to produce this picture the charge-coupled device had to move packets of approximately 400 electrons each through a centimeter of silicon without dispersion.

out video frames at different rates so as to match practical transmission-system bandwidths with standard television-display requirements.

Extension of the simple delay-line concept leads to other sampled-signal processing devices. If a delay line is fabricated with interim taps at which the signal can be sensed and fed back to earlier stages in such a way as to affect the transmission of the data, then this structure can be used as a filter. Such a structure can be conveniently configured as a band-pass filter where the resonant frequency of the circuit is a direct function of the clock frequency. An improvement in the signal-to-noise ratio to within a decibel of the theoretical maximum has already been achieved.

Matched filters find application in wide-spectrum communications and in radar to detect weak signals in high noise backgrounds. In such applications charge-coupled devices will complement acoustic-surface-wave devices, which generally are useful only for delays of less than 100 microseconds.

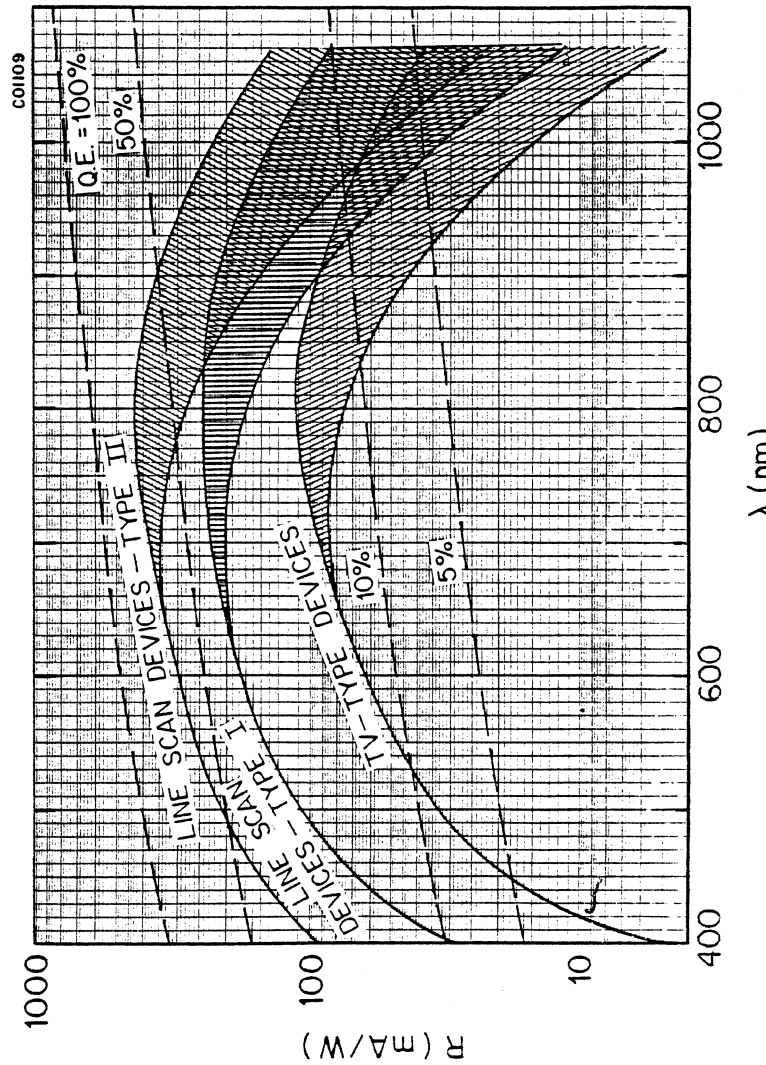
As mentioned above, a charge-coupled storage element is capable of storing a packet of electrons with a varying amount of charge, depending on the design and operating conditions of the charge-coupled unit cell. Nonetheless, there is no reason one cannot conceptually quantize the charge-handling ability of the cell and view the device as a binary digital element. For example, one can arbitrarily say that if a storage element contains a charge less than half the saturation charge, it contains a "zero," whereas if it possesses a charge greater than half the saturation charge, it contains a "one." In this way the storage element becomes a memory "bit" and a charge-coupled delay line can be made to serve the function of a digital shift register or serially accessible memory. Since this function can be performed by other technologies also, one must ask what charge-coupling has to offer. The answer is cost-effectiveness. A charge-coupled memory not only has all the advantages of a conventional semiconductor component (compatibility with other electronic circuit elements, no mechanical motion, low power and voltage, variable clocking rates and other similar features) but also offers a potentially low cost-per-bit ratio approaching that of a magnetic memory. This is a result of the inherent structural simplicity of the charge-coupled device. By virtue of this simplicity, memory arrays as large as a quarter of a million bits per component on a piece of silicon less than half an inch on a side can be envisioned.

In addition, the power necessary to sustain a charge-coupled memory device is very low since the storage element is not active. The power required to move the charge stored on one charge-coupled element to an adjacent element in a microsecond is approximately a microwatt. Moreover, in a properly organized memory it is not necessary to have all bits moving simultaneously. Thus a one-megahertz, one-megabit charge-coupled memory device would require a power of somewhere between a milliwatt and a watt to sustain it, excluding logic and other functions. The volume required for such a memory is less than that of a pack of cigarettes.

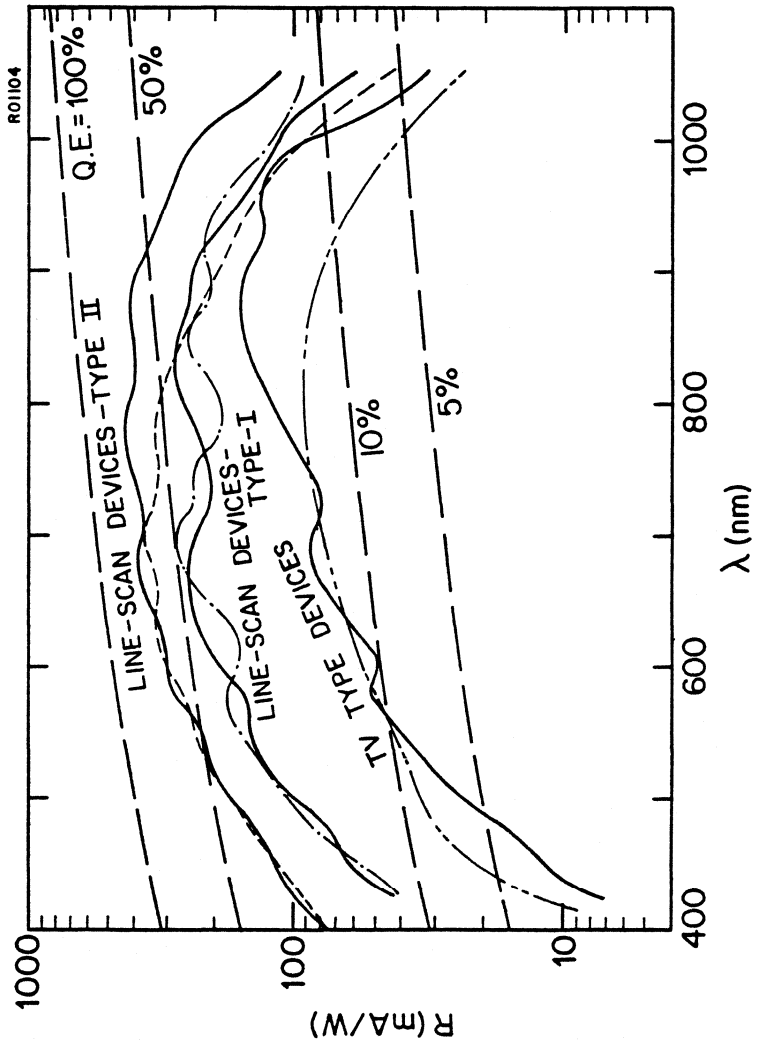
Another advantage lies in the fact that the charge-coupled device is basically analogue in nature. It is thus possible to store more than one data bit in each memory cell. This can be done by storing any one of a number of discrete levels of charge in each cell, thereby greatly increasing the information-packing density. For example, a 100,000-cell device capable of handling eight levels of charge is comparable to a 300,000-bit conventional memory. Such a memory chip would be of great value in digital-to-analogue and analogue-to-digital converters and other applications where multiple levels are achieved only by the addition of vast amounts of memory.

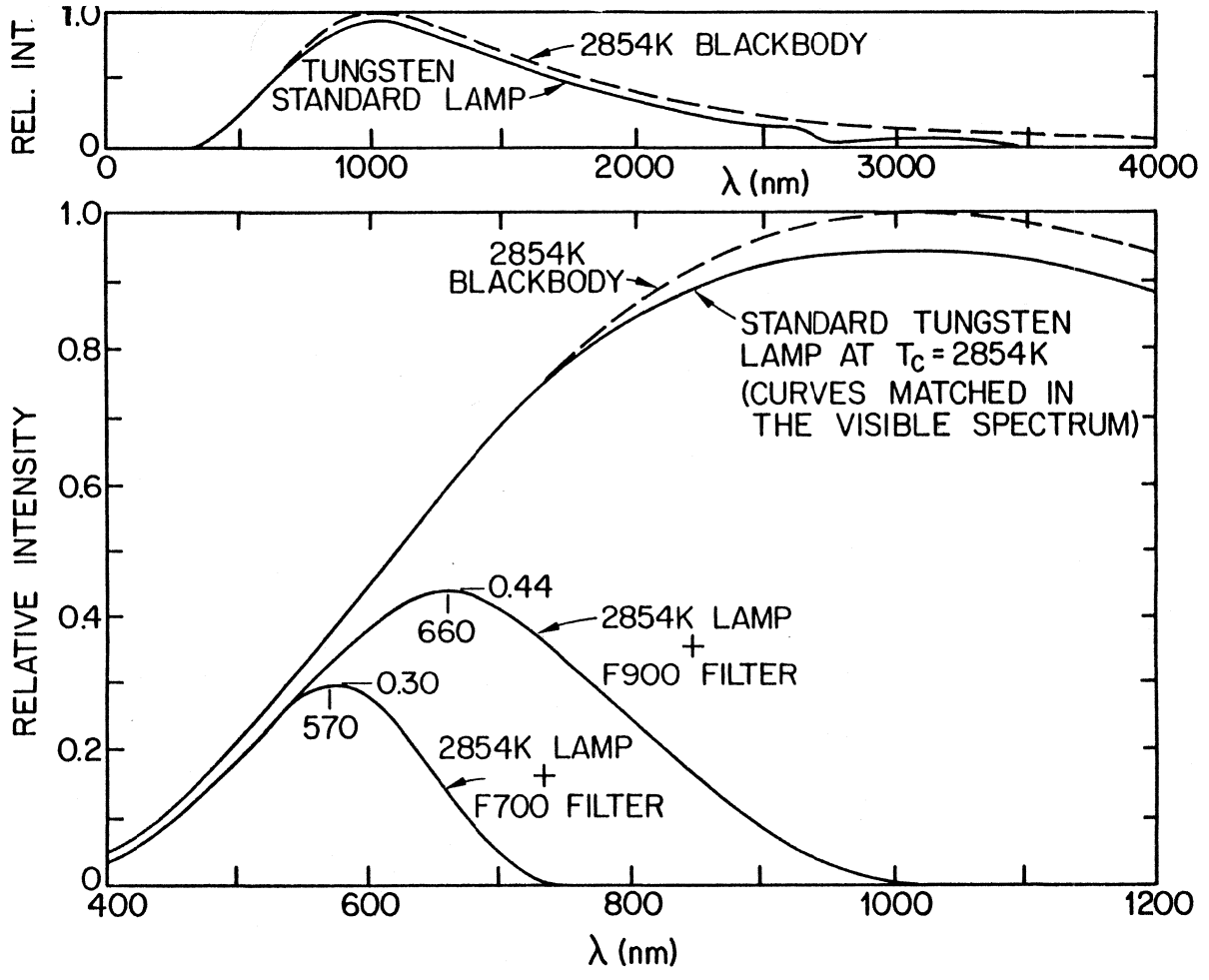
In view of these important prospective features of charge-coupled memory devices it appears that we are at the dawn of a revolution that will ultimately bring today's powerful digital computers directly into our everyday way of life. The charge-coupling concept, in short, is a major new innovation in semiconductor electronics. By virtue of its simplicity in design and fabrication, its high performance in terms of dynamic range and low power, and its high packing density and potentially low cost, the technology of charge-coupling will create major and unique new applications for semiconductors that will have a direct impact on our lives.

TYPICAL INTERNAL SPECTRAL RESPONSE (SMOOTHED)



TYPICAL INTERNAL SPECTRAL RESPONSE (UNSMOOTHED)





SPECTRA OF THREE BROADBAND LIGHT SOURCES

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TECHNICAL NOTE ON X-RAY IMAGING WITH FAIRCHILD CCD IMAGE SENSORS

BY R. H. DYCK

JUNE, 1981

X-ray imaging is conventionally done with either photographic film, X-ray phosphor screens viewed directly, or X-ray image converter tubes coupled to a vidicon-type of television camera. Solid state image sensors can provide several advantages over the conventional approaches. For example, by simply replacing the tube-type camera by a solid state camera one achieves the advantages of:

1) a distortion-free scanning raster,
2) an ultra-stable scanning raster, and
3) full digital control of the image readout, as is desirable for interfacing to digital systems

The above example can be implemented in two ways. One way is to use relay optics to image the output of the X-ray image converter tube onto the image sensor. Because sensitivity is generally quite important, the aperture of the lens should be approximately f/1.4 or larger, i.e., a smaller f/no. The other way is to use an image sensor with a fiber optics faceplace and a converter with a fiberoptic backplate. An improvement in sensitivity of 10 to 20 times has been achieved with this approach. In terms of numerical aperture (NA), the aperture of this type of coupling can be approximately 1.0; this is approximately equivalent to f/0.5.

Other approaches to X-ray imaging with solid state image sensors are: (1) to use an X-ray phosphor that is deposited directly on a fiber optics faceplate on the sensor, and (2) to let the X-rays excite the sensor directly. This last method is not recommended, however, since the X-rays incident on an image sensor, especially when it is powered, lead to degradation of the device similar to the way devices degrade due to any other form of high energy radiation such as gamma rays and high energy electrons. The effects include (1) increased dark signal, (2) decreased charge transfer efficiency, and (3) drift in optimum drive voltages. Depending on the particular type of radiation, the dose, the device and the temperature, any one of these effects may dominate.

Where X-ray imaging directly on the sensor is considered, the following information may be of value.

1) The attenuation depth in silicon varies strongly with X-ray energy. Above approximately 6 KeV, the characteristic attenuation depth (where the incident X-ray flux is attenuated 2.72 times) is greater than 30 μm. This situation results in relatively large crosstalk between photoelements, and also in the possibility of poor uniformity of response.

2) Continued exposure to X-rays, especially while under power, causes the device to degrade. Near room temperature, this will generally be detectable at 10^3 to 10^4 rads, and may make the device unusable at 10^5 to 10^6 rads. Annealling will restore proper performance to some degree, but since the best annealling only occurs at temperatures above the maximum recommended storage temperature, low-risk annealling treatments are not expected to help very much. Annealling assisted by ultraviolet irradiation may be considerably more effective.

3) Because good imaging is only expected for relatively low X-ray energies, and because the normal glass window on the image sensor strongly attenuates these low-energy X-rays, it is important to replace the glass window by a thin beryllium cover (of course, for ultraviolet-assisted annealling a beryllium cover would need to be removable).

4) Dosimetry. A rad is defined differently in silicon device investigations relative to the conventional definition for biological and health studies. For the latter, the definition is 100 ergs/gram in carbon. For silicon devices, it is 4.2×10^{13} electron-hole pairs/cm^3 in silicon. Another useful relationship in dealing with radiation effects in silicon devices is that it takes approximately 3.5 eV of energy, on the average for high energy radiation, to create one electron-hole pair in silicon.

5) Active area. Because the aluminum that shields the CCD registers from light is transmitting for X-rays, the registers may be stopped during an exposure, and the active area may be considered to include the registers. This situation results in oddly shaped element areas for line-scan imagers unless elements are paired. For paired elements, the resulting active element area is approximately 26 X 260 μm $\simeq$0.007 mm^2.

6) Example of an X-ray exposure and the resulting radiation dose. Assume 10 KeV radiation. Each X-ray photon will generate approximately 3000 photoelectrons. Of these, 2000 will be generated in the first 100 μm of depth. Assume all 2000 will be collected. Assume an average exposure of 50 X-ray photons per 26 x 260μm pixel. This will generate approximately 100,000 photoelectrons or approximately 10% of the saturation output voltage. This exposure expressed in radiometric units, is

$$\frac{(50 \text{ photons})(10^4 \text{eV/photon})(1.6\text{x}10^{-19} \text{ joule/eV})}{7\text{x}10^{-5} \text{ cm}^2} = 1.1\text{x}10^{-9} \text{ j/cm}^2.$$

The radiation dose seen by the upper portion of the device can be estimated as follows: assume a characteristic absorption length of 100 μm. The absorption coefficient is then one percent per micrometer. The excitation density at the top of the device and for the average exposure used in this example is then

$$\frac{(50 \text{ photons})(3000 \text{ pairs/photon})(0.01/\mu\text{m})(10^4 \ \mu\text{m/cm})}{(7\text{x}10^{-5} \text{ cm}^2)(4.2\text{x}10^{13} \text{ pairs/rad})} = 5.1 \text{ mRad}$$

Therefore, if one is careful not to expose the device unnecessarily to the X-ray source, it should be possible to take as many as 200,000 exposures before the significant degradation resulting from 10^3 Rads accumulated dose will occur.

Advanced charge-coupled device (CCD) line imaging devices*

David D. Wen
Fairchild Camera & Instrument Corporation
4001 Miranda Avenue
Palo Alto, California 94304

Abstract

The design and operation of a new high speed family of CCD line imaging devices are presented in this paper. The devices, CCD 133 and CCD 143, contain 1024 and 2048 photosites on 13 μm centers respectively. They are second generation devices having an overall improved performance compared with the first generation devices (CCD 121 and CCD 131) including higher sensitivity, enhanced blue response and lower dark signal. The devices also incorporate on-chip clock driver circuitry so that only two external clocks are required for their operation. Excellent performance has been obtained with up to 20 MHz data rate. The devices are designed for page scanning applications including high speed facsimile, optical character recognition, and other imaging systems which require high resolution, high sensitivity, and high speed.

Introduction

CCD line imaging devices manufactured by the Fairchild buried n-channel technology were first introduced commercially more than four years ago.[1] A second generation family of line imaging devices has recently been designed to replace them. The low speed second generation devices (CCD 122 and CCD 142), which operate up to 2 MHz data rate, have been described at the 1979 International Solid State Circuit Conference.[2] This paper reports the operation of the high speed second generation devices (CCD 133 and CCD 143) which are designed to operate up to 20 MHz data rate.

Device design and operation

The CCD 133/143 devices contain a line of 1024/2048 13 μm x 13 μm image sensor elements as shown by the block diagram in Figure 1. The photosites are separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Because there is no polysilicon gate layer over the photosites, the sensitivity is increased, particularly in the blue region of the spectrum. An N^+ region is diffused into the photosites to collect photogenerated electrons as illustrated in Figure 2. After an integration period is over, the transfer gate ϕ_X is turned HIGH to transfer the charge packets from the photosites into the two adjacent (inner) Analog Transport Shift Registers A&B. The transport registers are positioned 70 μm away from the photosites so that optical crosstalk is minimized. The N^+ diffusion region, illustrated in Figure 2, also provides conductive coupling[3] between the photosite and the shift register regions. As a result, charge transfer across the 70 μm distance can be accomplished in less than 30 ns.

The CCD shift registers are constructed with two polysilicon layers with self-aligned ion-implanted barriers.[1] A buried-channel ion implantation is employed so that the CCD shift registers operate in the bulk-channel mode. Excellent charge transfer efficiency can be obtained with this structure at clock frequencies in excess of 30 MHz. One-and-half phase clocking[4] is employed so that only one external clock (ϕ_T) is required for the shift register operation. A gated-charge integrator output amplifier is provided for each of the two analog transport shift registers, as illustrated in Figure 3. The gated-charge integrator contains two MOS source follower stages with a switching transistor positioned between the two stages so that sampled-and-held output waveforms are obtained. The output impedance of the gated-charge integrators is designed to be 750 ohms in order to drive an external capacitive load (approximately 10 pF) at up to 10 MHz clock rate. Since the two gated-charge integrators alternately detect charge packets transferred from the two shift registers, a combined output video data rate of 20 MHz can be obtained. On-chip MOS circuitry, illustrated in Figure 4, generates all the required clock waveforms to operate the output amplifiers. The MOS clock drivers are designed with bootstrap feedback capacitors for high frequency operation. The two sample-and-hold clock waveforms (Ψ_{SHA} and Φ_{SHB}) are each 35 ns in width to assure proper operation at 10 MHz clock rate (20 MHz data rate).

* Manufactured under U. S. Patent 3,931,674.
Other patents pending.

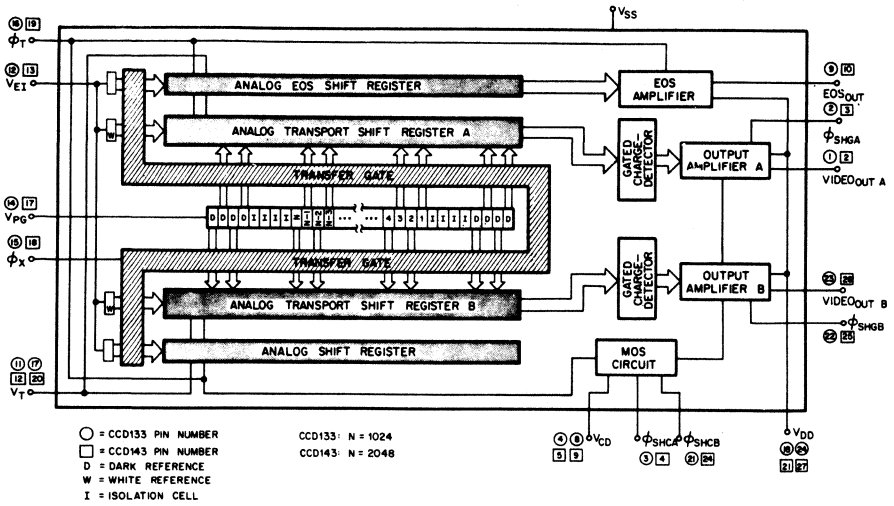

Figure 1. Device block diagram.

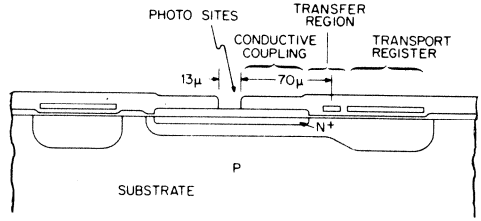

Figure 2. Cross-section of photosites and shift register.

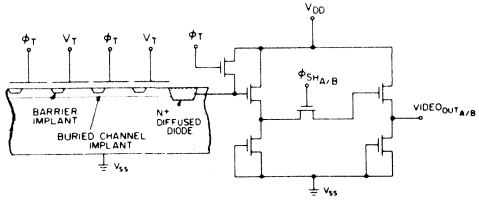

Figure 3. Output amplifier schematic.

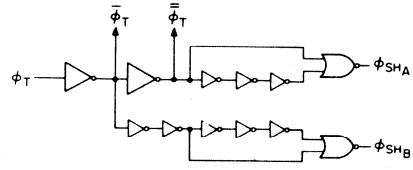

Figure 4. On-chip MOS circuit.

In addition to the regular photosites, the devices also contain four dark reference cells at each end of the array as illustrated in Figure 1. These dark reference cells are constructed the same as the regular photosites except that they are kept dark by the covering of opaque aluminum metallization. They provide an accurate dark reference level in the device output waveforms so that external signal processing such as DC restoration can be performed. Figure 1 also shows isolation cells situated between the dark reference cells and the regular photosites. These isolation cells are reverse-biased diodes which are used to eliminate optical crosstalk between the regular photosites and the dark reference cells.

An electrical injection circuit is provided at the beginning of each of the transport shift registers as indicated in Figure 1. A cross-sectional diagram of the electrical injection circuit is shown in Figure 5. It can be seen that the magnitude of the charge injected is determined by the same well and barrier potentials which determine the saturation level of the shift registers. These electrically injected signals (called white reference cells) track the device saturation level with respect to amplifier gain and temperature effects as well as process variations. These charge packets are injected at the end of the exposure period when ϕ_X is turned HIGH. They are then transported along the readout shift registers and appear at the output amplifiers after the regular photo-generated charge packets. The white and dark reference levels can be used to achieve automatic gain control in many optical system applications.

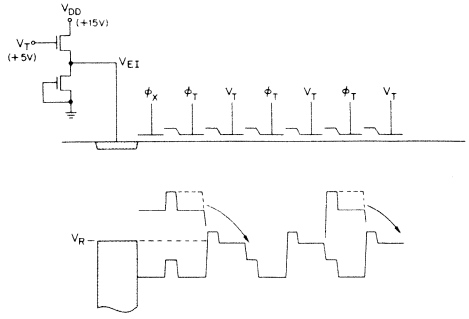

Figure 5. Electrical injection structures for the white reference level.

As illustrated in Figure 1, a total of four CCD shift registers are provided on the device. The signal charge packets from the photosites are transported along the two inner shift registers. The two outer shift registers are used to collect charge that may be generated in the field so that the signal charge packets are not affected. An electrical injection structure identical to the white reference circuit is also provided for one of the outer shift registers. The detection of this charge packet by the output amplifier indicates that the readout of a line of video data has been completed. The use of this end-of-scan (EOS) output eliminates the need for external counter chains.

The devices are designed to operate with only two external clocks (both with 12 volt amplitude). ϕ_T controls the output data rate, and ϕ_X controls the exposure time interval. Due to the fast transfer achieved with the N^+ diffusion region discussed before, ϕ_T is a continuous clock which does not need to be interrupted during the ϕ_X transfer period. Typical output waveforms of the device are shown in Figure 6. It can be seen that both outputs are sampled-and-held, and contain dark and white reference levels as discussed previously.

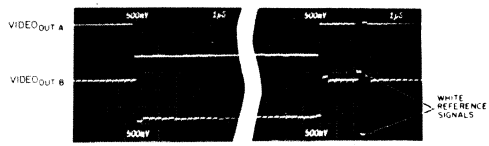

Figure 6. Device output waveforms.

Typical device performance characteristics are summarized in Table I. Under the standard test condition of 25°C, 5.0 MHz data rate and 1 ms integration time, the device provides 2 volt saturation output and less than 10 mV of dark signal. Temporal noise measured without illumination is typically 400 μV RMS, resulting in a 5000 : 1 dynamic range. Excellent charge transfer efficiency of better than 0.99999 per transfer is obtained. The device operates with a single 14 volt, 22mA DC power supply. Maximum output video data rate is 20 MHz. Typical spectral response and MTF (modulation transfer function) measurements are shown in Figures 7 and 8.

Table 1. CCD 133/143 Typical Performance Characteristics

Saturation output voltage	2.0 V
Responsibility	3.0 V/μJcm^{-2}
Max. dark signal*	7.0 mV
Photoresponse nonuniformity*	± 10%
Charge transfer efficiency	0.99999
Temporal noise (in dark)	400 μV RMS
Dynamic range	5000 : 1
Output impedance	750 Ω
Power dissipation	380 mW
Max. output data rate	20 MHz

* Measured at 25°C, 1 ms integration time, light source is 2854°K + BG 38 + WBHM filters (480 nm to 650 nm wavelength)

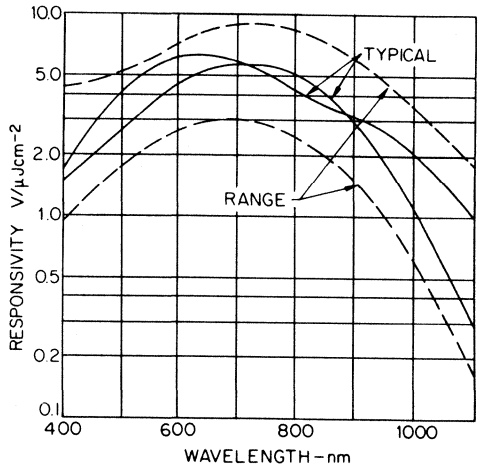

Figure 7. Spectral response measurement.

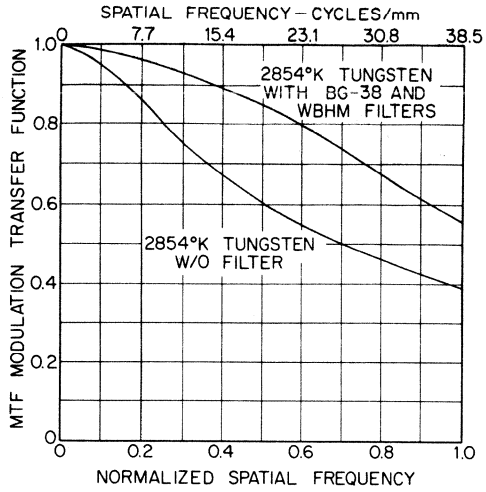

Figure 8. MTF measurement.

Conclusion

The design and performance of the CCD 133 and CCD 143 have been discussed in this paper. The devices contain 1024 or 2048 photo-sensing elements on 13 μm centers. Only one DC power supply and two external clocks are required for their operation. Excellent results have been obtained up to 20 MHz output data rate.

The 1024 sensing elements of the CCD 133 provide 120-line-per-inch resolution across an 8-1/2 inch page, the 2048 sensing elements of the CCD 143 provide an 8-line-per-millimeter resolution across a 256 millimeter page for standard Japanese facsimile use. The devices should find applications in facsimile, optical character recognition and other imaging systems where high resolution, high sensitivity and high speed are desired.

Acknowledgments

The author wishes to thank Will Steffe for many helpful discussions, Sampath Ranganathan for on-chip MOS circuit design, and Richard Youden and Denice Denton for device characterization.

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TECHNICAL NOTE

PREDICTED EFFECTS OF HIGH-POWER AND HIGH-ENERGY OPTICAL IRRADIANCE ON CCD IMAGE SENSORS

This technical note describes the predicted effects of large concentrations of radiant optical energy on Fairchild CCD image sensors - such as might occur with a laser or a solar image. It should be understood that these are only predictions; we do not know of actual instances of such damage. All of the effects are thermal; that is, this technical note only deals with heating effects due to dc or pulsed radiation that is concentrated in some definable way. The emphasis will be on worst-case conditions.

As a point of reference let us first consider how much heating will typically occur when a device is uniformly irradiated near saturation at some common integration period. We will only treat the case of monochromatic light at a central wavelength, namely, 600nm, and we will only consider one typical device, namely, the CCD133. The area of the dark ceramic header (90% absorbant) is approximately $4.5cm^2$. At the data sheet test condition of 1ms integration period, with the device near saturation the radiant power absorbed by the device can be estimated to be, based on data sheet information:

$$0.9\ (0.4\mu J/cm^2)\ \ (4.5cm^2)/10^{-3}s = 1.6mW$$

(The saturation energy density of $0.4\mu J/cm^2$ was calculated by dividing the typical saturation voltage of 2.0V by the typical spectral responsivity at 600 nm of $5V/\mu J/cm^2$.)

A rough estimate of thermal resistance of the package is $10^oC/W$. Therefore the estimated rise in temperature is:

$$1.6mW\ (10^oC/W) = 0.016^oC$$

If the radiation is confined to the area of the silicon chip ($0.2cm^2$), which has an average absorbtance of only about 20%, the corresponding values are:

$$0.2\ (0.4\mu J/cm^2)\ \ 0.2cm^2)/10^{-3}s = 8\mu W$$

and

$$8\mu W\ (10^oC/W) = 0.00016^oC$$

Let these two temperatures be our point of reference. Next let us consider several representative specific examples of high energy optical irradiance.

Case 1. The sun is focused on the device. In one specific scenario an F/2 lens forms an image of the sun 2.3mm in diameter on the CCD133 chip. The luminous intensity of the solar image is:

$$\frac{\pi\ (1.6 \times 10^9 \text{ lumen/steradian. m}^2)}{4F^2}$$

$$= \frac{3.14\ (1.6 \times 10^9)}{4\ (2)^2} = 3.2 \times 10^8 \text{ lux}$$

Using our recommended 700 nm infrared blocking filter, one lux equals approximately 0.33mW/cm^2, giving a power density of 100W/cm^2 and a total incident power of 3.2W. Taking the absorbtance to be 20% (as we did above for the mostly aluminized chip) the total absorbed power is approximately 0.64W and the temperature rise of the chip above the ambient is approximately

$$0.64\text{W}\ (10^{\circ}\text{C/W}) = 6^{\circ}\text{C}$$

Since the device is rated at 125°C maximum, there is no danger at all of harming the device, assuming there is adequate control of the ambient temperature.

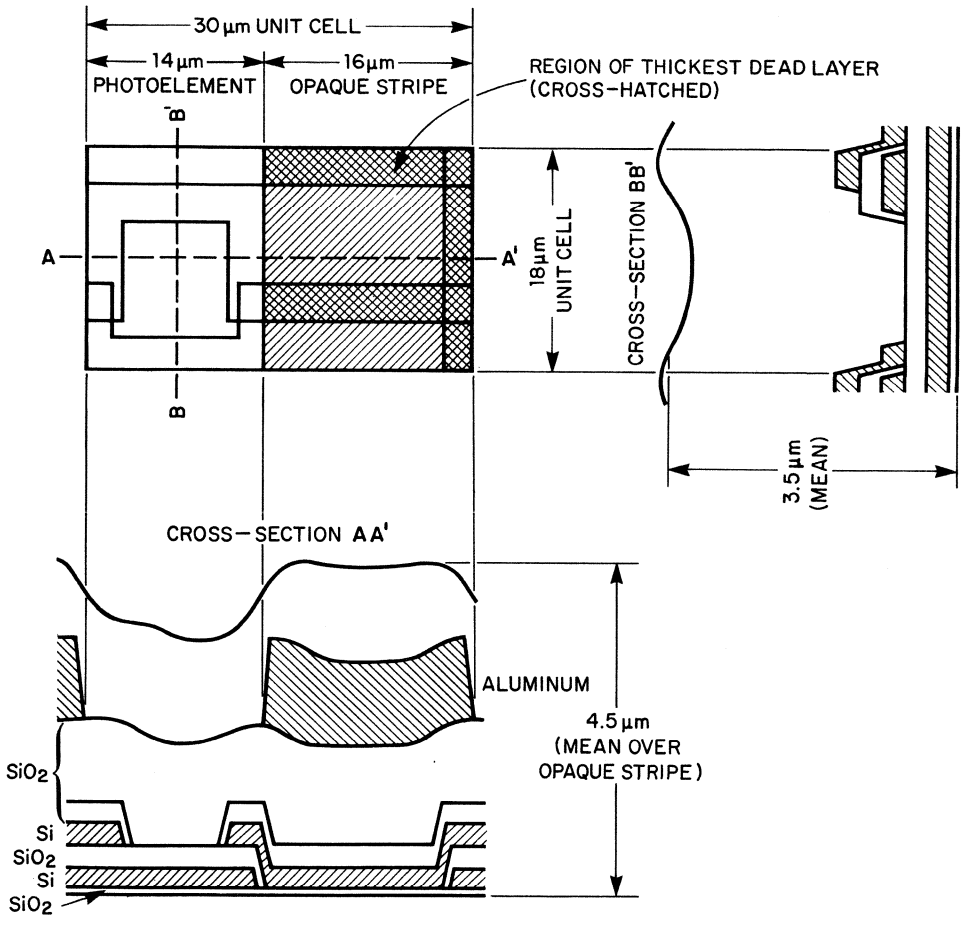
Case II. A laser spot 10μm in diameter is focused on the chip. The question is: What are the power and pulsed energy limits before something gets too hot? For this case, it is useful to think of the silicon chip as a large heat sink on which is an insulating glass layer 1 - 3μm thick, and an aluminum layer 1μm thick. The aluminum can absorb power faster than it can spread laterally and downward to the single crystal silicon heat sink. If the aluminum layer reaches a temperature of 450°C for even very brief times like a few minutes, it is possible to damage the device. (This occurs at the aluminum - silicon contacts.) For laser pulses less the 20-50ns, the power would not spread significantly outside the 10μm spot and one can calculate the incident energy required to heat that amount of aluminum by $450 - 25 = 425^{\circ}$C. In addition to the information we already have, we need the heat capacity of aluminum, which is $2.4\text{J/cm}^3{}^{\circ}\text{C}$. The critical energy level is then

$$\frac{2.4\text{J/cm}^3{}^{\circ}\text{C}\ \ (10^{-4}\text{cm})\ (425^{\circ}\text{C})\ \ (8\text{X}10^{-7}\text{cm}^2)}{0.1} = 0.8\mu\text{J}$$

For pulses longer than 20 - 50ns, this critical energy will increase because the heat has time to spread, but simple quantitative predictions are probably not reliable because of the complexity of the chip structure.

General Observation. Since the silicon chip can withstand 125°C indefinitely and 450°C for very brief periods of time, and since CCD devices typically saturate at illumination levels that heat the device by less than 0.1°C, it is clear that there is at least a 1000:1 safety margin above saturation before damage will occur.

DEAD-LAYER STRUCTURE OF THE STANDARD CCD 222 RELATIVE TO HIGH-ENERGY PARTICLE-SENSING APPLICATIONS



Intensified CCD Camera Uses Fiber-Optic Coupling

Microchannel plates are imaging devices which are sensitive to charged particles and energetic photons. Originally developed for use as the amplifying element in military night vision systems, the microchannel plate is now finding its way into microscopes, oscilloscopes and solid-state cameras.

When used in CCD cameras, the increase in sensitivity obtainable depends to some degree on the type of illumination source since the spectral response of the intensifier is significantly different from the CCD. However, in approximate terms, the sensitivity can be increased by factors as high as 1,000. The minimum faceplate illumination can be reduced also, by a factor of three. Fairchild's CCD3000I intensified camera is based on the company's 3000 camera and uses an 18mm diameter wafer-type image sensor in its design.

A schematic diagram of the front end of the camera is shown in Figure 1. In the basic CCD camera, the light from the lens passes through a thin glass window and forms an image directly on the CCD. In this intensifier-CCD camera, the image is focused on the front of the image intensifier which then produces an equal sized intensified image at the back surface. This image is transmitted to the CCD by means of a fiber-optic block that is in direct optical contact with the chip.

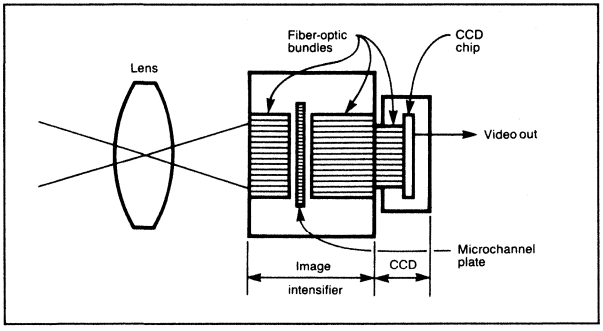


FIGURE 1: Block diagram of the front end of the intensifier CCD camera.

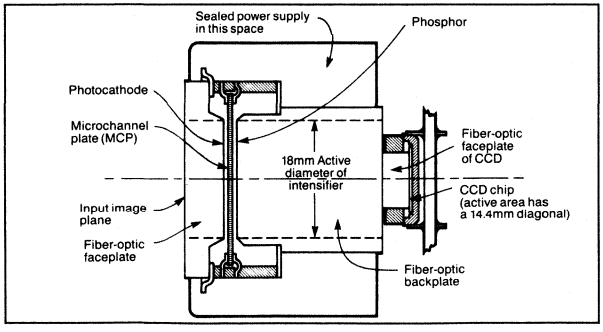


FIGURE 2: Detailed drawing of the intensifier and the fiber-optic CCD.

This system is shown in more detail in Figure 2. The intensifier is a small active diameter (18mm) wafer-type intensifier made by Varo Electron Devices (Garland, TX). It is known as a wafer-type of intensifier because of the small distance from the photocathode to the phosphor which is approximately 0.1in. Gain is achieved within a microchannel plate where each microchannel acts as a high gain electron multiplier.

Focus is maintained through the structure by the proximity of the members and by high applied voltages that minimize the time that the emitted electrons spend in the spaces on either side of the microchannel plate. This minimizes spreading of electrons due to initial lateral velocities. Fiber optics are used for the backplate to allow fiber-optic coupling with its attendant high optical efficiency.

The CCD image sensor is a 488 × 380 element device, modified by replacing the normal thin glass window with a fiber-optic faceplate. The fiber-optic faceplate rests against the CCD chip. The faceplate and CCD chip are optically coupled with oil which is approximately 2μm thick. The faceplate is held in place relative to the CCD chip with the aid of a surrounding frame. A photograph of the fiber-optic CCD is shown in Figure 3.

The fiber-optic structures are made up of highly transparent fiber cores that are 4-6μm in diameter and an interstitial glass that is slightly optically absorbant. Depending on the refractive indices of the two glasses, the core regions have the property of total internal reflection for light incident over large solid angles. On-axis transmittances of the individual fiber-optic blocks are typically 80 to 90%. This fiber-optic CCD is held against the intensifier by spring-loading the PCB in which it is mounted; again, the interface has an optical grade of oil.

R.H. Dyck
Fairchild CCD Imaging
Palo Alto, CA

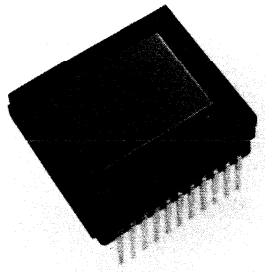


FIGURE 3: The CCD image sensor with its fiber-optic faceplate.

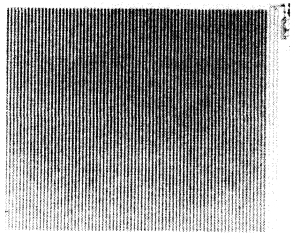


FIGURE 4: A photograph of a portion of the image sensor with its fiber-optic faceplate.

In view of the small fiber size compared to the size of the unit cell of the CCD ($18 \times 30\mu m$) one would expect only a small amount of image degradation and, in fact, very little is observed. Typically, there are 20 to 25 fibers per $18 \times 30\mu m$ unit cell with a few of these not being useful because they only illuminate the opaque portion of the unit cell containing the vertical CCD register cell. The high quality of the image transmitted through the fiber-optic block is shown in the device photograph (Figure 4). The vertical, lighter shade bars are aluminum strips on $30\mu m$ centers. Some of the preamplifier structure is visible through the fiber-optic faceplate in the upper right hand corner.

The quality of imagery produced by the CCD/fiber-optic faceplate combination is illustrated in Figure 5. For this picture, an image was formed on the front surface of the fiber-optic faceplate with an ordinary camera lens.

Performance

The sensitivity of the camera is determined by the quantum efficiency of the photocathode, the intensifier gain, the CCD responsivity at the intensifier phosphor mean wavelength and the CCD noise or CCD background signal. Under some conditions, the sensitivity will be limited by the shot noise in the primary photoelectron stream. For the smaller features in the image, sensitivity will also be limited by the MTF of the imaging system.

The response spectrum of the photocathode is shown in Figure 6. This type of photocathode is called the S-20 extended red. Because of its high quantum efficiency in the red (600-700nm) and the near IR (700-800nm) compared to other available photocathodes, it is well suited to night vision applications. For example, where there is moonlight, this photocathode is desirable for its ability to sense a broad portion of the spectrum and thereby generate more total photocurrent.

For a second example, where there is some small amount of incandescent lighting, the red and IR responsivity of this photocathode takes advantage of the high output from lighting in that part of the spectrum. The broadband responsivity is conveniently described in terms of photometric units using a standard 2854°K tungsten light source. The typical value is $200\mu A$ per lumen.

The gain of the image intensifier may be expressed in more than one way. The most common way is to give the photometric output per unit of photometric input. This takes into account the photocathode responsivity. Manufacturers give typical values of between 7000 to 15,000 footlamberts/footcandle. Here unity gain means that if one viewed the phosphor screen on-axis, the output would be one lumen per unit solid angle for every pi (3.14) lumens incident on the photocathode. Since the angular distribution out of the fiber-optic backplate is more or less ideal ("Lambertian"), this is approximately equivalent to one lumen out per lumen in. Of course, this measure of gain requires that the type of light source be specified; in this case, it is again a 2854°K standard tungsten source.

Another way to describe the gain

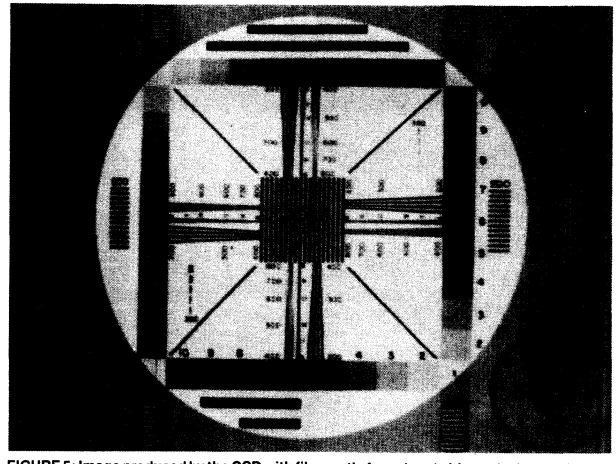


FIGURE 5: Image produced by the CCD with fiber-optic faceplate (without the intensifier).

would be to give the number of photons emitted from the intensifier (at the mean wavelength of the phosphor, namely, 560nm) per electron emitted from the photocathode. This measure of gain may be calculated to be 25,000 to 55,000.

Unfortunately, the intensifier camera has to suffer losses in quantum efficiency both in the photocathode and in the CCD, with the result that the predicted net increase in responsivity is of the order of 2000. As already noted, the reduction in the minimum illumination level onto the front end photosensitive surface, where the picture qualities appear most similar, has been found to actually be approximately 1000 times.

The ability of the intensifier camera to faithfully reproduce details in scenery is limited in two different ways, just as it is in any video camera: by the Nyquist-limit resolution and by the MTF. The Nyquist limit resolution is a property of the CCD and is not altered by the intensifier. The MTF is the product of the MTF of the CCD by itself and that of the intensifier by itself. As can be seen in Figure 7, the major MTF loss occurs in the intensifier. Nevertheless, there is useful MTF out to at least 25 line pairs/mm in the intensifier alone ($\approx$ 5% MTF) and by the same measure, there is useful resolution in the CCD intensifier camera out to at least 23 line pairs/mm. Since the CCD raster measures 8.8mm vertically, this provides a useful resolution in the vertical direction of at least 400 TV lines. In the horizontal direction, the MTF is greater than 15% at the Nyquist limit.

Overall camera performance is illustrated by some night scenes recorded with one of the cameras (Figures 8 and 9). An f/2.5 zoom lens was used wide open. A nearly full moon was still rather low in the sky; the light meter read 0.35 lux at the car in Figure 8 and 0.15 lux where the man is standing in Figure 9. One-fifth of a second exposures integrate noise to approximately the same degree as is perceived by a typical observer.

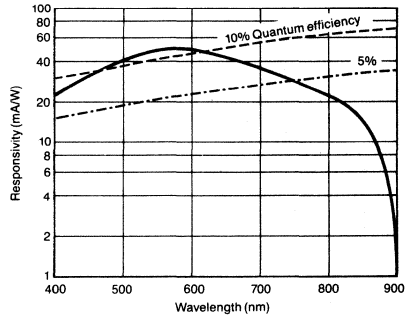


FIGURE 6: Photocathode responsivity (Varo-S20/extended red).

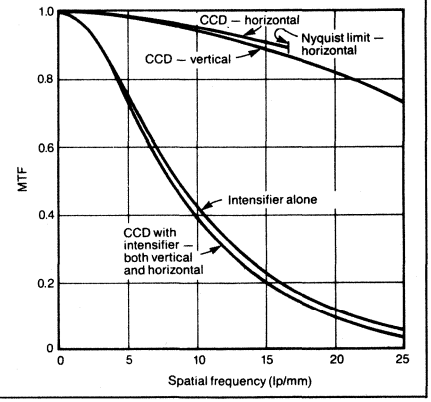


FIGURE 7: MTF of the CCD222, the intensifier alone and the combination of the two.

FIGURE 8: Parking lot in moonlight.

FIGURE 9: Night scene where a building shaded the scene from moonlight.

At 0.35 lux, the parking lot scene is imaged with a sufficiently large S/N ratio that detail is observable over a broad range of gray levels. At 0.15 lux, a few gray levels can be discerned in the man's clothing, whereas the foliage is essentially too dark to see. In the 0.35 lux scene (Figure 8), the illumination level near the car is predominately from the moon with perhaps 20 or 30% coming from a nearby light.

There is a self-limiting behavior in the image intensifier: when the total intensifier output emitted (electron) current reaches the limit of the built-in power supply, the supply voltage drops so as to keep the average image intensity from the intensifier more or less constant. In the camera, at least for night scenery like that in Figures 8 and 9, the signal level in the CCD stays near the saturation level and only occasionally might a bright light in the scene cause the CCD to bloom. Because of this self-limiting feature, the camera behaves as if it had AGC and offers a good S/N ratio over several decades of average scene brightness.

Fiber-optic coupling

The use of fiber-optic coupling between the output phosphor layer of the intensifier and the CCD provides a coupling efficiency estimated to be in the neighborhood of 60%. Because the fiber optics are of the type designated numerical aperature (N.A.) 1.0in, the fraction of the omnidirectional light incident on the fibers themselves which exits from those fibers is close to 80%. Then each of the two fiber-optic plates (the intensifier backplate and the CCD faceplate) has a core fill factor that is about 85%. This gives a resultant efficiency of approximately $8 \times 0.85 \times 0.85 = 0.58 \doteq 60\%$.

If, instead, a relay lens had been used, it would have been possible to improve the resolution somewhat by imaging the entire 18mm phosphor screen onto the CCD, but the coupling efficiency would have been considerably less.

For example, if an f/1 lens had been used as the relay lens, the half-angle of the cone of accepted light would have been approximately 15° and the fraction of light accepted from the nearly ideal (Lambertian) phosphor light source would have been approximately $\sin^2 15° = 0.065$. This is essentially a factor of ten lower than the figure for the fiber-optic case, and this estimate needs to be reduced further due to the imperfect transmission coefficient of any real lens.

In addition to this disadvantage of a lens coupler, there are the disadvantages of size and weight. This may add four inches or more to the camera length. For the case of a small primary lens, the weight of the front end portion of the camera might have been nearly doubled had a relay lens be used.

Acknowledgements

The author would like to thank Lee Ruzicka for major assistance in the designing of the prototype camera, in minimizing its noise, and in the characterization of the camera. The author would also like to thank Howard Murphy for many helpful discussions during the development of the camera.

Vision Interface Processor Links CCD Cameras to Multibus

Increases in productivity from non-contact industrial inspection, robotics and factory automation systems have created a demand for systems which require vision. Due to variations in requirements for vision systems, many task functions are not available within standard turnkey products, and users are often forced to construct their own systems.

There are three steps necessary to solve vision problems. Image formation is usually accomplished by using a video camera for image data collection. More and more this involves solid-state cameras which are attractive because of zero lag and geometric distortion properties as well as size, ruggedness and reliability. After image formation, usually obtained as an analog signal at video frame rates, a means of acquiring the image and digitizing the information into machine readable form is required. For this purpose commercially available frame grabbers are commonly employed. Finally, processing and analysis of the image data results in a decision and system response. In the last step system builders rely on the powers of microcomputers and software algorithms tailored to the particular task involved.

Allan P. King
Fairchild CCD Div
Palo Alto, CA

Image formation

Based on the CCD222, an NTSC compatible 488 × 380 element buried channel CCD image sensor, the CCD3000 camera is a small, rugged camera suited for industrial environments. The camera enclosure consists of a sense head containing the sensor which may be remoted from the rest of the control electronics contained in the camera body. The sealed sense head is designed to tolerate high acceleration and vibrations which may be found on a moving robot arm.

RS–170 video output is obtained by supplying ±15 and +5V DC power to the back of the camera control unit (Figure 1). The camera allows the user access to many of the internal timing signals produced by the camera as well as three different options for camera input timing. The camera may operate asynchronously under control of its own internal 14.318 MHz crystal at a 30Hz frame rate. It may also be operated externally via either an external master clock input permitting variable frame rates of 0.2 to 45Hz or through horizontal and vertical drive inputs allowing frame rates over the range of 15 to 45Hz.

The master clock generates CCD timing signals on the control unit logic board. These signals are passed through the drive board, which creates the voltages needed to drive the sensor, and onto the sense head to create the sensor horizontal drive signal. This is a high frequency clock signal which must be situated near the CCD. Sensor video from the CCD is sampled, and then fed back to the control unit where composite sync and blanking are added to generate the RS–170 video. There is an IR absorbing filter placed behind the lens that limits light wavelengths hitting the array to the visible spectrum which results in an increased contrast transfer function.

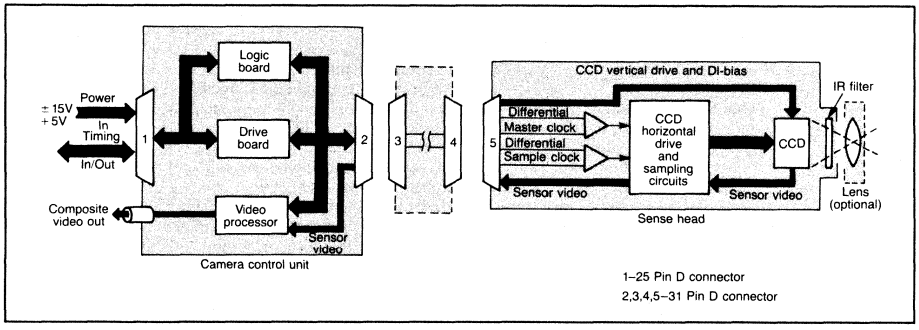


FIGURE 1: Fairchild's CCD3000 camera block diagram.

Image acquisition and analysis

The VIP100 is a Multibus formatted video processing card which can be used as a frame-grabbing memory for camera to computer interfacing or as a sophisticated stand-alone processor. As shown in Figure 2, data acquisition and single board processing are accomplished with use of an on-board F9445 16-bit mi-

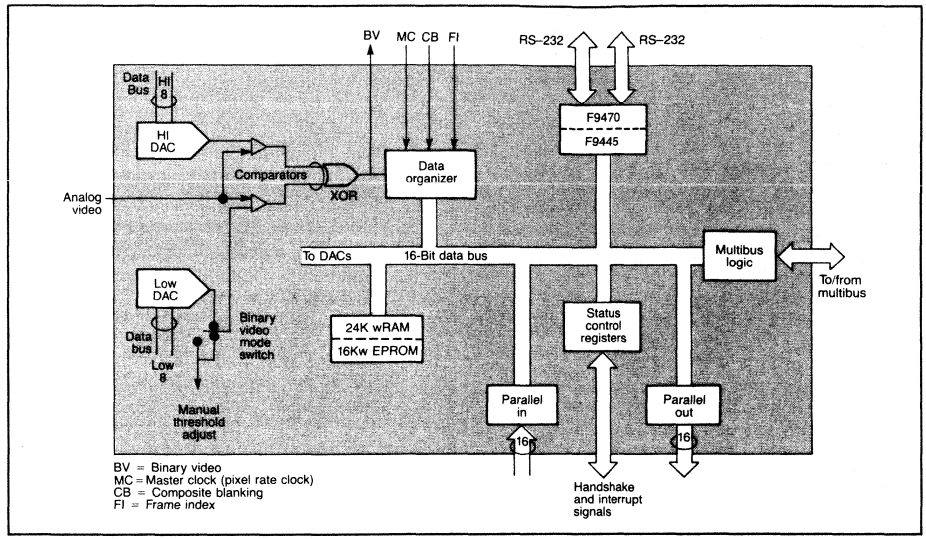


FIGURE 2: On the vision interface processor data acquisition and single board processing are accomplished with an on-board F9445 16-bit microprocessor.

croprocessor in combination with an F9470 console controller. The F9445 was selected to obtain high-speed processing necessary for real time data acquisition from the camera and for high-speed processing of the acquired data.

Under control of the F9445, converted digital data may be acquired through either the Multibus, a 16-bit parallel port or either of two RS-232C ports. The F9470 which controls the RS-232C ports operates in two modes: virtual console control and I/O service. In console control, communication with the F9445 is controlled by the F9470. In I/O service mode, the F9470 acts as a serial I/O controller, interfacing the RS-232C I/O ports to the VIP100.

Image acquisition begins with either standard RS-170 or non-standard video. Also required are a master clock, composite blanking and a frame index clock which are provided by the CCD3000 camera. Input analog data is converted into binary two programmable 8-bit DACs. The output from the DACs are exclusive ORed and formed into 16-bit words by a 16-bit SIPO shift register (Data Organizer). From the register, the F9445 loads the words into the resident memory. The two RS-170 fields are stored in a non-interlaced format. Once in memory the video information is available for on-board processing, or for transfer to a host processor.

The F9445 processor and F9470 console controller are supported by 24k words of static RAM (16k words for image data storage, 8k for user programs) and space for 16k words of 2732 EPROM (Figure 3). External memory may also be expanded in any combination of RAM or ROM up to 1M bytes using the Multibus.

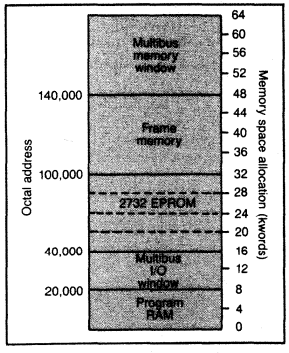


FIGURE 3: Memory map of the VIP100. One frame from a CCD3000 camera requires 11.5k words of memory.

Of the 16k words EPROM space, 4k words are used for storage of an absolute assembly language (AAL) monitor program, Fairchild's customizing SEEBUG and a BASIC program, the PEPBASIC-45.

Software support

The VIP100's SEEBUG monitor program, incorporated in EPROM, is a debugging tool that provides commands for troubleshooting assembly-langugae programs, setting the DAC threshold values and controlling image acquisition. PEPBASIC-45 also in EPROM is an optimized form of BASIC which can be used to develop customized applications programs.

Through use of a development system, such as the Fairchild System-1, large program editing, assembling/compiling, and general file storage and handling may be accomplished.

Cross assembler software packages may be obtained for creating machine-executable programs in formatted form.

The VIP100 may also be tied to other computers and is capable of uploading and downloading programs via one of the two RS-232C ports.

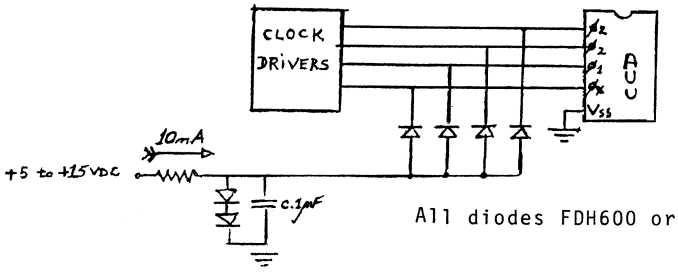
Charge Injection

Every CCD device input pin has a Gate Protection Structure which includes a diode from the input to the (grounded) substrate V_{SS}. The diode is reverse-biased during normal operation ($V_{in} \geq V_{SS}$). Negative (transient) input voltages ($V_{in} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chips.

If sufficient charge is injected, it will accumulate in the CCD Analog Shift Register(s) and/or the Photosites near the injecting Gate Protection Structure(s). Injected charge which accumulates in the photosites will typically result in an apparent bell-shaped increase in the Background Dark Signal (FWHM =20-100 pixels wide) near the injecting Gate Protection Structure. Injected charge which accumulates in an Analog Shift Register will result in an apparent uniform increase in that register's Background Dark Signal, creating a noticeable increase in apparent Register Imbalance ("odd/even") of the Background Dark Signal.

The susceptability to charge injection sufficient to increase the Background Dark Signal varies significantly from device to device. It is not possible to select devices with "low" susceptability. However, devices with low Dark Signal are typically more susceptable than devices with high Dark Signal.

Sufficient charge to appear as increased Background Dark Signal may be injected by negative transient voltages <4 ns long. Since these transients can not be detected by oscilloscopes with less than 250-500 MHz bandwidth, a system which appears to be free from negative transients on a 200 MHz scope may still be prone to charge injection. The recommended method to eliminate charge injection is the following diode clipper-circuit.



All diodes FDH600 or equivalent.

The diode should be within an inch of the CCD if possible.

CCD TECHNICAL INSIGHTS

Element Anti-Blooming

A crucial performance feature of any camera system concerns the overload or blooming characteristic. Highlights in a scene (such as an automobile-bumper reflection) often reach 20 to 50 times the saturation exposure level of the sensor. Some mechanism must be used to maintain undistorted imagery over the non-highlighted portions of the scene. In CCD sensors, this mechanism, known as element anti-blooming, is accomplished by bleeding away overload signal charge through drain lines adjacent to each photoelement.

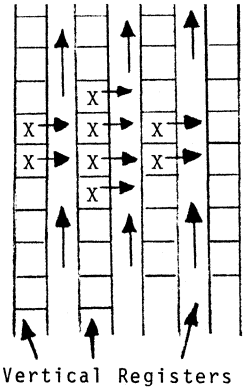
The element anti-blooming structure developed by CCD imaging provides blooming control at more than 50 times the saturation exposure level and maintains anti-blooming control up to the optical crosstalk limit of the vertical shift registers. The Figure shows the same subject as reproduced by area image sensors with and without element anti-blooming. Element anti-blooming capability enhances the value of CCD area image sensors as potential replacements for vidicon tubes in broadcast cameras.

Image Without and With Element Anti-Blooming

CCD TECHNICAL INSIGHTS

Optical Crosstalk

With our new EAB devices, the problem of blooming is adequately controlled up to about 50 times the saturation charge level. However, as the charge level increases in the photosites, another phenomenon occurs that appears similar to blooming, but is less noticeable at lower charge levels. This effect is due to optical crosstalk of photo-electrons from the photosite into the vertical shift registers. (See Drawing)



X = Illuminated Photoelements In Light Spot

Picture a small spot of light focused on the area array. Charge is building up in the illuminated photoelements. Some fraction of this charge can leak under the shift register barrier and be scanned upwards appearing in the device output. It appears on the monitor as a faint vertical line as wide as the light spot (much like a faint blooming). Note the primary difference between blooming and crosstalk is that blooming is an overflow of a full photosite and all excess electrons flood the registers, whereas crosstalk is a small percentage of signal electrons that wander under the shift register barrier which does not extend very deeply into the silicon. Crosstalk builds gradually as signal charge is increased. As one might expect, the longer the light wavelength (towards the infrared), the worse the crosstalk effect. This is due to the fact the longer wavelength, lower energy photons,

generate charge more deeply in the silicon where the photo-element fields are weak and hence the charge is more apt to wander in to the adjacent shift register.

The magnitude of actual crosstalk varies depending on wavelength but overall crosstalk is on the order of 12% or so in an average device. It can vary though from 7 or 8% to 22% depending on the device. Therefore, at about 8 times the saturation charge level, while the anti-blooming structure is still effective, the device will saturate with the optical crosstalk signal. This means that the blooming control is really only effective up to the optical crosstalk limit. After that point, image data is lost anyway.

CCD TECHNICAL INSIGHTS

Electrons vs. Voltages

Usually, when one talks about the output from a CCD image sensor or camera, they refer to so many volts or millivolts of output. It may be in regards to the saturation voltage, an output voltage, photoresponse non-uniformity, dark signal non-uniformity, responsivity or noise etc. All our data sheets talk in terms of voltages out. Some find it useful, however to talk in terms of charge, or electrons of signal rather than referring to voltages because it is electrons that are actually being moved about in the device. The voltage appears only as a result of convering this charge in the output amplifier.

The voltage at the output is linearly proportional to the number of electrons being converted. As a rule of thumb, our line scan CCD's output 1.0-1.5μV per electron of charge received, and the CCD222 about 2.5-2.7μV per electron. One may use this "scaling factor" to convert voltages back to electrons. For instance:

Parameter	Linear Imager		Area Imager	
	Volts	Electrons	Volts	Electrons
V_{SAT}, Q_{SAT}	1.5V	1,000,000e^-	0.8V	300,000e^-
V_{OUT}=50% V_{SAT} OR Q_{SAT}	750mV	500,000e^-	400mV	150,000e^-
NOISE (rms) (In Dark)	.4mV	270e^-	.16mV	60e^-

CCD TECHNICAL INSIGHTS

DARK SIGNAL vs TEMPERATURE CALCULATIONS:
WORST-CASE* ERROR IF DOUBLING RATE IS NOT MEASURED

	Dark Signal Correction Factor [Ratio of $\frac{DS(T_1)}{DS(T_o)}$] When:			Measure $DS(T_o)$ • Assume K=10°C The difference between actual $DS(T_1)$ and calculated $DS(T_1)$ will be: When:		
$(T_1 - T_o)$	K=5°C	K=10°C	K=15°C	K=5°C Actually	K=15°C Actually	Units
+0.1°C	1.014	1.007	1.005	+0.7%	-0.2%	Actual % of DS (T_1)
+0.2	1.028	1.014	1.009	+1.4%	-0.5%	"
+0.5	1.072	1.035	1.023	+3.6%	-1.2%	"
+1.0	1.149	1.072	1.047	+7.2%	-2.3%	"
+2.0	1.320	1.149	1.097	+14.9%	-4.5%	"
+3.0	1.516	1.231	1.149	+23.1%	-6.7%	"
+4.0	1.741	1.320	1.203	+32.0%	-8.9%	"
+5.0	2.000	1.414	1.260	+41.4%	-10.9%	"
+10.0	4.000	2.000	1.587	+200.0%	-20.6%	"
+20.0	16.000	4.000	2.520	+400.0%	-39.7%	"

*Worst Case is that the Dark Signal Doubling Interval will not be less than 5°C nor greater than 15°C.

Definitions:

$$DS(T_1) = DS(T_o) \bullet 2^{[(T_1-T_o)/k]}$$

Where $DS(T_o) \overset{def.}{=\!=}$ A component of dark signal at temperature T_o.

$K \overset{def}{=\!=}$ "Doubling Rate" of that dark signal component.

CCD TECHNICAL INSIGHTS

CHARGE TRANSFER EFFICIENCY (CTE) CALCULATIONS

Assume that the CCD photosites are uniformly illuminated. Also assume that every shift register element has the same charge transfer efficiency. Then:

$$\text{CTE (per 1 transfer)} = \left(1 - \frac{n\varepsilon}{\text{Vout}}\right)^{(1/i)}$$

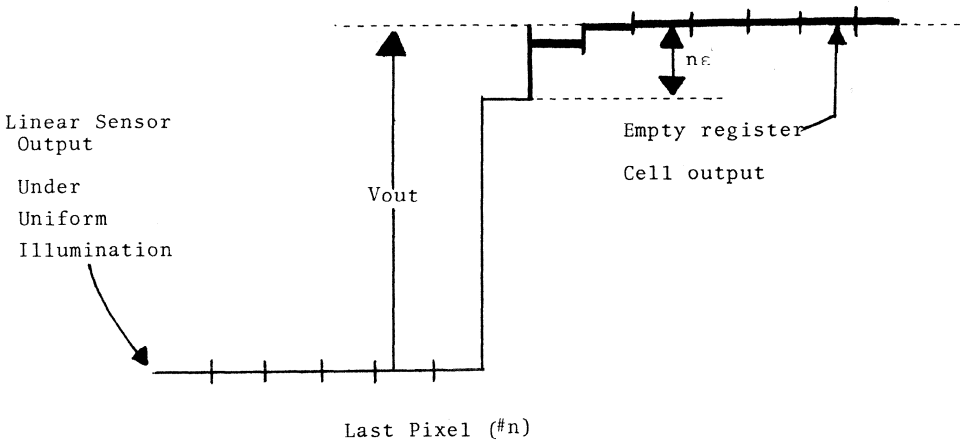
$n\varepsilon$ and Vout are defined on the following page; "i" is the total number of shift register elements (transfers) between pixel #n and the output amplifier. Note: each shift register bit consists of two elements; two transfers are required to move a charge packet through one shift register bit. Also, as shown below, there are more bits than the theoretical sensor length due to some extra bits (dark reference, prescan etc.) in the line of video.

The table below lists $n\varepsilon$ versus CTE for each type of linear imaging device.

CTE (/1 Transfer	CCD111 i=259	CCD133 i=1,035	CCD143 i=2,059	$n\varepsilon$ UNITS
0.999 999	$n\varepsilon$ 0.03%	$n\varepsilon$ 0.10%	$n\varepsilon$ 0.21%	% of Vout
0.999 995	0.13	0.52	1.02	"
0.999 990	0.26	1.03	2.04	"
0.999 980	0.52	2.05	4.03	"
0.999 970	0.77	3.06	5.99	"
0.999 960	1.03	4.06	7.91	"
0.999 950	1.29	5.04	9.78	"
0.999 940	1.54	6.02	11.6	"
0.999 930	1.80	6.99	13.4	"
0.999 920	2.05	7.95	15.2	"
0.999 910	2.30	8.89	16.9	"
0.999 900	2.56	9.83	18.6	"

CTE

Definition of nε and Vout



Q - What does "quantum efficiency" mean?

A - Quantum efficiency in an imaging CCD is a term referring to the efficiency with which incident photons are converted to hole-electron pairs. If each incident photon is converted to one hole-electron pair, the quantum efficiency is 100%. If more hole-electron pairs are created than entering photons, we have a multiplication effect and the quantum efficiency is >100%. If fewer hole-electron pairs are created than incident photons, the Q.E. is <100%.

Q - What are the quantum efficiencies of our CCD imaging devices.

A - Acutal Q.E. curves for our CCD devices are shown on pages 185 and 186 of the CCD data book.

Line Scan Devices- TypeII devices include our second generation photosite structure (photogate moved to the side of the photosite) Devices include the CCD112, 122, 123, 133, 134, 143, 145 and 151. The Q.E. for these parts approaches 70%.

Line Scan Devices- Type-I devices include our first generation photosite structure. (Photogate covering the photosite) The only device of this type is the CCD111. The Q.E. for this part approaches 40%.

TV - Type devices include all current CCD area imaging arrays; CCD222,231, Robotics Sensor. The Q.E. of these devices is ≅15%. The reasons for the low Q.E. on area arrays are twofold:

1) We have polysilicon layers covering the photosites as in the case of Type-I linear array

2) We have ≅60% of the array covered by non-absorbing aluminum which prevents photons from reaching the shift register portion of the array. (Note that the 40% active area when multiplied by 40% Q.E. of Type-I linear arrays gives you about 15% Q.E. overall).

CCD TECHNICAL INSIGHTS

Q - How is it that we can minimize the size of an array and still maintain high resolution? After all, our CCD222 has a 14mm diameter, which is a little large to be traveling in may orifices of the body. Many endoscopy applications require diameters of less than 5mm.

A - A drastic decrease in size may be obtained by altering the basic structure of the CCD interline transfer type device we currently produce. In an ILT device, charge is transferred from the photosite area into an adjacent opaqued shift register. The register is opaqued to prevent image smearing during readout due to light hitting the register. If the light could be turned off during readout, the registers would not have to be opaqued. If they did not have to be opaqued, the shift register stages themselves could be used for imaging. And if the registers can image, we can get rid of the photosites, thereby greatly decreasing chip size.

Since in an endoscopic application there is total darkness surrounding the array, we can image by strobing the subject periodically and readout during darkness. This is ideal for the type of device just described. Therefore, to achieve the smallest size possible, we take the shift register stage down to the smallest dimension currently possible (about 10µm x 10µm) and eliminate the photosites. We can achieve resolutions this way of 300 plus elements per side and still be within the 5mm diameter limit. Color can be achieved by time sharing the device strobing among different colors, and reproducing the image via external circuitry.

CCD TECHNICAL INSIGHTS

Q- What are the length of die tolerances and pixel size tolerances on our linear imaging devices? What is the center-to-center pixel spacing error?

A- The "pitch" of a CCD linear image sensor is defined as the center-to-center photosite spacing. The pixels and thus the pitch are defined initially on the die by the first masking operation.

The first source of pitch inaccuracy is due to the mask. The masks are "written" during the maskmaking process by an electron beam. Due to machine limitations, the e-beam writes in "blocks" about 0.25-0.32 inches long, which is 500-630 pixels per block at 13µm pitch. The pixel at the edge of each block may be ±0.125µm too wide or narrow. Within the block, the pitch of any two adjacent pixels is accurate within ±0.016µm. However, the total cumulative pitch error is ±0.00006µm/pixel*, which is equivalent to ±0.065µm total for 1,024 pixels at 13µm pitch. (i.e., the CCD133) (All data above is worst-case.)

The second source of pitch inaccuracy is expansion or contraction of the silicon die between first mask in wafer fabrication and window glass cover in packaged device assembly. The silicon die length changes slightly during each high-temperature processing step. Solder die-attached devices - all current production products, except the CCD123 - are 0.030µm/pixel to 0.059µm/pixel shorter after seal/cover than the theoretical pitch of exactly 13µm. For the CCD133 (1,024 pixels, 13µm pitch, solder die attach), this totals 3-6µm/array. This contraction is linear along the array.

*Cumulative pitch error is equal to the total length block error divided by the number of pixels in the block.

CCD TECHNICAL INSIGHTS

Q - What light sources are recommended for use with CCD's?

A - Any light source in the visible spectrum is recommended for use with CCDs. Usual choices are "daylight flourescent", or filtered tungsten. Tungsten has some IR content which should be filtered out for best results. Monochromatic lasers are also quite acceptable in the visible spectrum. Remember, the reason IR light is not recommended is that optical crosstalk between pixels increases with wavelength and image clarity (MTF) goes down. Silicon does however, have a good sensitivity below 1.1μm and for certain applications where low contrast is acceptable, some near IR light sources may be used.

Q - How long an integration time is necessary to acquire an image using a CCD?

A - The answer depends strictly on the wavelength and intensity of the light. At a fixed wavelength, it depends solely on intensity. (See Responsivity Curves for Sensitivity vs. Wavelength). Integration time is not as important as exposure. Exposure =.integration time x light intensity. Therefore, very short (on the order of nanoseconds) integration times are possible with an intense enough light.

Q - How intense may the light be before the device is damaged?

A - Damage to the device does not occur until the device aluminum light shield is actually melted by heat generated from the light source. Generally the source has to be very intense to melt the aluminum shield. To give you a benchmark, direct sunlight hitting the device focused through an F/2 lens and concentrated on a 2.3mm diameter spot causes only a 6°C increase in chip temperature. The aluminum shield may withstand 125°C temperature indefinitely and up to 450°C for brief periods of time.

CCD TECHNICAL INSIGHTS

Q - I've purchased a CCD3000C with a 50mm lens from Fairchild. I have an object 1 meter in length and want to resolve the entire object with a resolution of at least 1mm. The 1024 elements of the CCD1300C, when viewing a 1 meter object, give me that resolution. I want to know how far away the camera must be from the object to achieve this resolution.

A - Using the following two lens equations, the working distance from the object may be calculated.

$$\frac{1}{f} = \frac{1}{ID} + \frac{1}{OD} \quad \text{and} \quad M = \frac{OL}{IL} = \frac{OD}{ID}$$

f = focal length in mm

ID = image distance (from lens to array) in mm

OD = object distance (from lens to object) in mm

M = magnification

OL = length of object in mm

IL = length of image to be focused on array in mm.

Step 1. Determine the needed magnification of the system.

OL = 1 meter

IL = 13μm x 1024 elements = 13.312 mm
(to achieve maximum resolution)

Therefore $$M = \frac{OL}{IL} = \frac{1000mm}{13.312mm} = 75.12$$

Step 2. Rearrange equations to solve for desired parameter.

Since $\frac{1}{f} = \frac{1}{ID} + \frac{1}{OD}$ and $M = \frac{OD}{ID} = \frac{OL}{IL}$ then

$$ID = \frac{OD}{M}, \quad \frac{1}{f} = \frac{1}{\frac{OD}{M}} + \frac{1}{OD} = \frac{M}{OD} + \frac{1}{OD} = \frac{M+1}{OD}$$

Therefore OD = f(M+1) = 50mm (75.12+1)=3806mm
= 3.806 meters

IMPORTANT NOTE: The image distance (ID) need never be determined to solve the equations. One doesn't need to know the distance from the lens to the array itself.

CCD TECHNICAL INSIGHTS

Q - What is the difference between an "R" and a "C" camera?

A - The industrial "R" camera, standing for ruggedized, is a piece of a line scan camera system. The camera includes logic and drivers to run the CCD and provides raw video from the two sides of the high speed (two output) arrays. The user must provide power, two clocks, a video combiner (not trivial) to combine the two video outputs together as well as any video processing electronics he desires to use.

The camera is intended as a lower cost system "component" for smart users, or users who need multicamera systems and are willing to design all the control and/or video processing electronics.

The commercial "C" camera includes everything the "R" camera includes plus more. (There is a slight performance advantage in the "R" camera which permits data rates to 20MHz instead of 10MHz as in the "C".) The "C" camera also includes a power supply, generation of all clock signals a video combiner for those sensors requiring it, AGC circuitry in the video output and an analog-to-binary converter with adjustable threshold for computer compatibility. The pixel locator option may also by used with the "C" camera, but not with the "R" without substantial circuit design.

The "C" camera is intended for those less familiar with the operation of CCD's and is a more complete system. It should be most customers first line scan camera purchase.

CCD TECHNICAL INSIGHTS

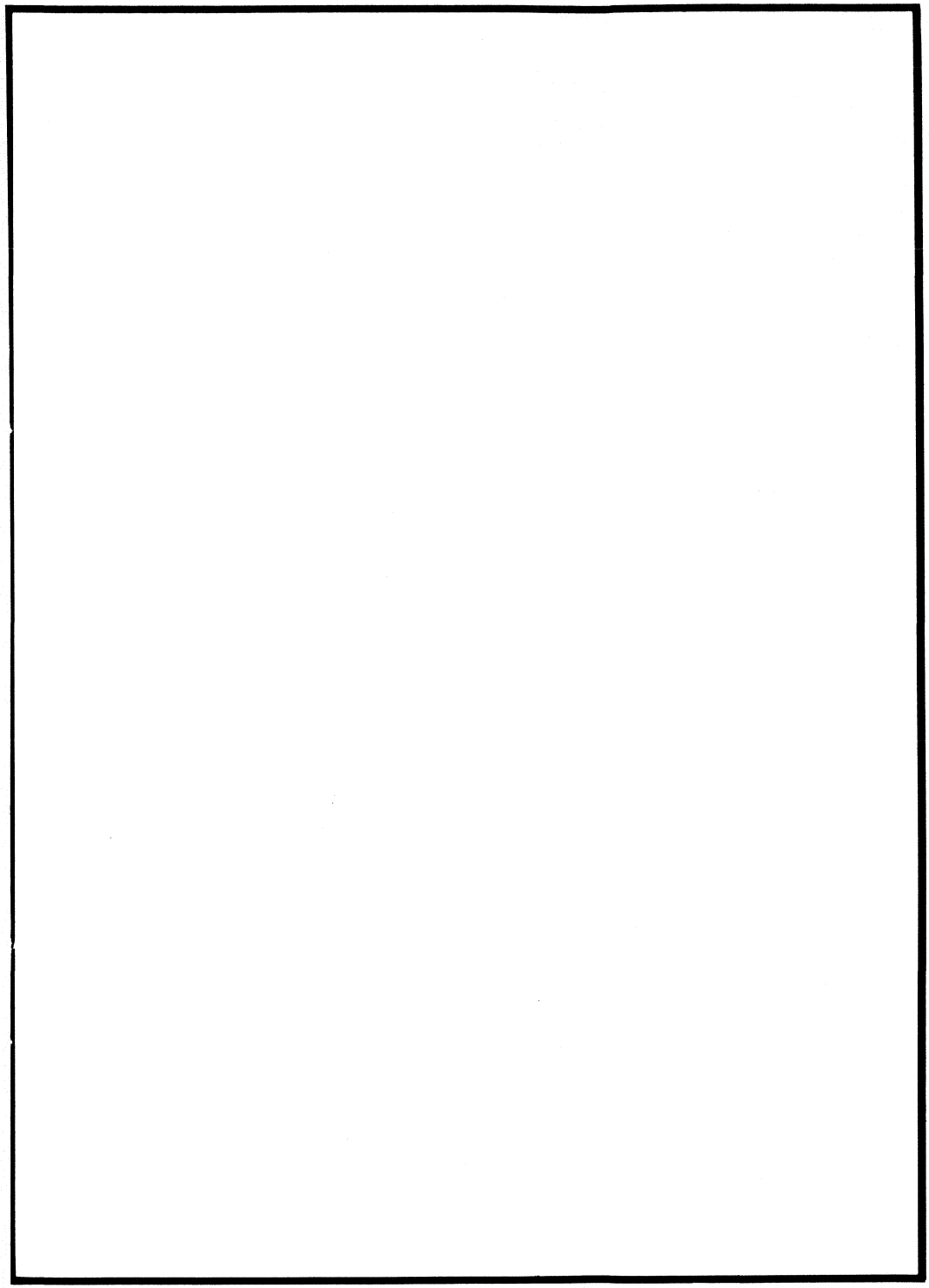
Q - What frame rates restrictions are there on the CCD3000 camera?

A - The CCD3000 camera was designed to run in three timing modes as shown below

1) Internally, under control of a 14.318MHz crystal. In this mode the frame rate is fixed at 30Hz.

2) Externally, under control of a user supplied clock input that bypasses the internal crystal. The resulting frame is equal to 30Hz times the ratio of the input clock frequency to 14.318MHz. The range of frame rates achievable due to internal circuitry limitations (not device limitations) is from 0.2Hz to 45Hz.

3) Externally, in the genlock mode using horizontal and vertical drive inputs. Although designed to allow synchronization of frame rates very close to the NTSC standard of 30Hz, the CCD3000 will allow external control of frame rates from ≈15Hz to ≈31Hz, using genlock inputs.



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Telex: 134273

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A-1120 Wien
Tel: (0222) 83.56.46-0
Telex: 131532

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B-1070 Bruxelles
Tel: (02) 523.62.95
Telex: 6121646

Rodelco S.A.
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Tel: (02) 216.63.30
Telex: 61415

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Tel: (40) 81.65.65
Telex: 51992

Rodelco B.V. Electronics
P.O. Box 6824
NL-4802 HV Breda
Tel: (76) 78.49.11
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92160 Antony Cedex
Tel: (1) 666.21.12
Telex: 250067

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Telex: 300021

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Telex: 610237

Est
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Telex: 960929

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Telex: 120257

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Feutrier
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Telex: 940930

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10 Bis, Avenue de Crimée
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Tel: (40) 48.09.44
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Telex: 530089

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Tel: (56) 39.51.21
Telex: 540030 Ref. 522

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Tel: (42) 82.16.41

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Tel: (1) 609.91.36
Telex: 260042

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Telex: 440076

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Telex: 721437

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Oslo 10
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Telex: 51024

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Fairchild Semiconductor S.A.
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D-7250 Leonberg
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Telex: 330522

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Via Francesco Saverio Nitti 11
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SCANDINAVIA

Fairchild Semiconductor AB
Svartensgatan 6
S-11620 Stockholm
Sweden
Tel: (08) 44.92.55
Telex: 17759

SWITZERLAND

Fairchild Semiconductor GmbH
Baumackerstr. 46
CH-8050 Zürich
Tel: (01) 311.42.30
Telex: 823285

UNITED KINGDOM

Fairchild Semiconductor Ltd.
230 High Street
Potters Bar,
Herts.
Tel: (0707) 511.11
Telex: 262835

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